

# Compal Confidential

## NEW71/91 M/B Schematics Document

### Intel Arrandale Processor with DDRIII + Ibex Peak-M NV N11P-GV2H

2009-12-23

REV : 0 . 1

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				Size Custom	Document Number NEW71/91 M/B LA-5893P Schematic Date: Wednesday, December 23, 2009
				Rev 0.1	Sheet 1 of 56

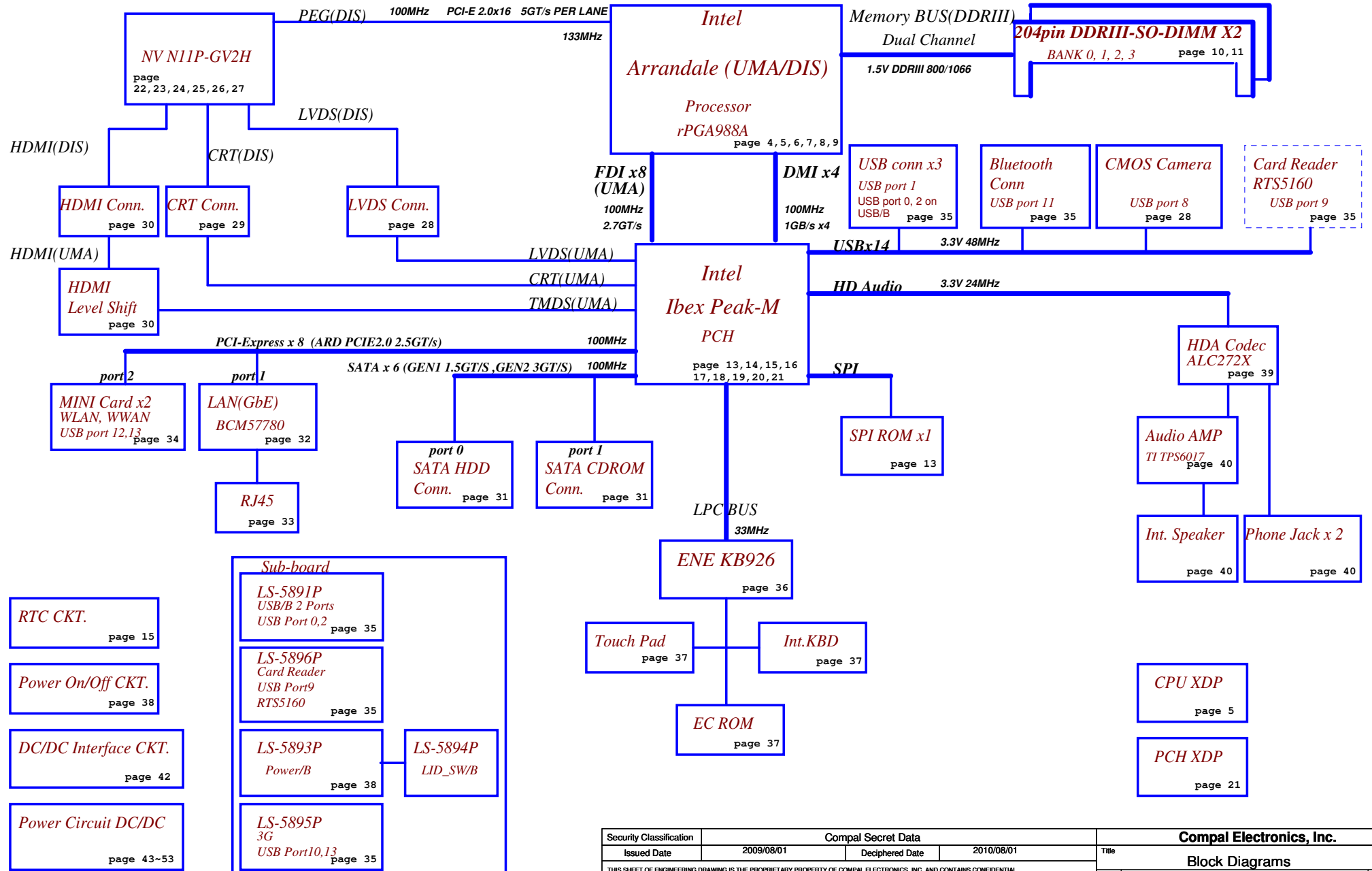
# Compal Confidential

Model Name : NEW71/91

File Name : LA5893P

Fan Control  
page 41

Clock Generator  
IDT: 9LVS3199AKLFT  
Realtek: RTM890N-631-VB-GRT  
133/120/100/96/14.318MHZ to PCH  
page 12



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				Date	Friday, December 18, 2009
				Sheet	2 of 56
				Rev	NEW71/91 M/B LA-5893P Schematic 0.1

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Config	
NEW71 SKU DISCTETE ONLY	BT@,3G@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,XDP@
NEW91 SKU DISCTETE ONLY	BT@,3G@,DIS@,DIS ONLY@,NonSG@,91@,X7621@,XDP@

VRAM BOM Config  
X7621@: X76198BOL21 ALT. GROUP PARTS 1G SAM  
X7622@ X76198BOL22 ALT. GROUP PARTS 1G HYN

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA Only	UMA ONLY@
Discrete	DIS@
Discrete Only	DIS ONLY@
VRAM	X76@
Switchable	SG@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
Unpop	@
XDP	XDP@
NonSG	NonSG@
NEW71	71@
NEW91	91@

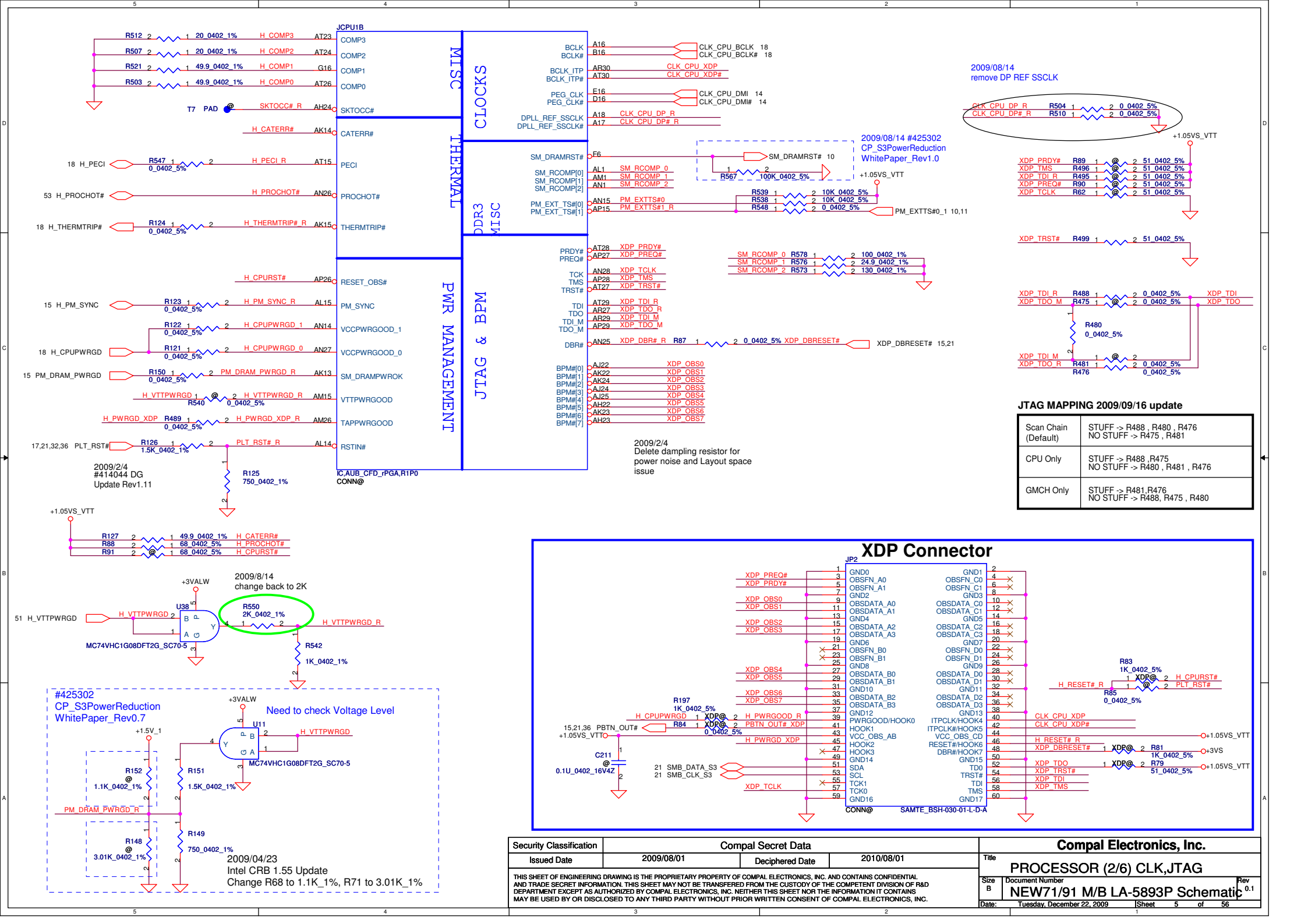
VRAM P/N :  
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)  
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO! )

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Card Reader
	UHCI5	10	SIM Card
		11	Blue Tooth
	UHCI6	12	Mini Card(WLAN)
		13	Mini Card(GPS)

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Size B	Document Number			Rev	
	NEW71/91 M/B LA-5893P Schematic			0.1	
Date:	Tuesday, December 22, 2009	Sheet	3	of 56	





10 DDR\_A\_D[0..63]  
10 DDR\_A\_DM[0..7]  
10 DDR\_A\_DQS[0..7]  
10 DDR\_A\_MA[0..15]

JCPU1C

DDR A D0 A10 SA\_DQ[0]  
DDR A D1 C10 SA\_DQ[1]  
DDR A D2 C7 SA\_DQ[2]  
DDR A D3 A7 SA\_DQ[3]  
DDR A D4 B10 SA\_DQ[4]  
DDR A D5 D10 SA\_DQ[5]  
DDR A D6 E10 SA\_DQ[6]  
DDR A D7 A8 SA\_DQ[7]  
DDR A D8 D8 SA\_DQ[8]  
DDR A D9 F10 SA\_DQ[9]  
DDR A D10 E6 SA\_DQ[10]  
DDR A D11 E7 SA\_DQ[11]  
DDR A D12 E9 SA\_DQ[12]  
DDR A D13 B7 SA\_DQ[13]  
DDR A D14 E7 SA\_DQ[14]  
DDR A D15 C6 SA\_DQ[15]  
DDR A D16 H10 SA\_DQ[16]  
DDR A D17 G8 SA\_DQ[17]  
DDR A D18 K7 SA\_DQ[18]  
DDR A D19 J8 SA\_DQ[19]  
DDR A D20 G7 SA\_DQ[20]  
DDR A D21 G10 SA\_DQ[21]  
DDR A D22 J7 SA\_DQ[22]  
DDR A D23 J10 SA\_DQ[23]  
DDR A D24 L7 SA\_DQ[24]  
DDR A D25 M6 SA\_DQ[25]  
DDR A D26 M8 SA\_DQ[26]  
DDR A D27 L9 SA\_DQ[27]  
DDR A D28 L6 SA\_DQ[28]  
DDR A D29 K8 SA\_DQ[29]  
DDR A D30 N8 SA\_DQ[30]  
DDR A D31 P9 SA\_DQ[31]  
DDR A D32 AH5 SA\_DQ[32]  
DDR A D33 AF5 SA\_DQ[33]  
DDR A D34 AK6 SA\_DQ[34]  
DDR A D35 AK7 SA\_DQ[35]  
DDR A D36 AF6 SA\_DQ[36]  
DDR A D37 AG5 SA\_DQ[37]  
DDR A D38 AJ7 SA\_DQ[38]  
DDR A D39 AJ6 SA\_DQ[39]  
DDR A D40 AJ10 SA\_DQ[40]  
DDR A D41 AJ9 SA\_DQ[41]  
DDR A D42 AL10 SA\_DQ[42]  
DDR A D43 AK12 SA\_DQ[43]  
DDR A D44 AK8 SA\_DQ[44]  
DDR A D45 AL7 SA\_DQ[45]  
DDR A D46 AK11 SA\_DQ[46]  
DDR A D47 AL8 SA\_DQ[47]  
DDR A D48 AN8 SA\_DQ[48]  
DDR A D49 AM10 SA\_DQ[49]  
DDR A D50 AR11 SA\_DQ[50]  
DDR A D51 AL11 SA\_DQ[51]  
DDR A D52 AM9 SA\_DQ[52]  
DDR A D53 AN9 SA\_DQ[53]  
DDR A D54 AT11 SA\_DQ[54]  
DDR A D55 AP12 SA\_DQ[55]  
DDR A D56 AM12 SA\_DQ[56]  
DDR A D57 AN12 SA\_DQ[57]  
DDR A D58 AM13 SA\_DQ[58]  
DDR A D59 AT14 SA\_DQ[59]  
DDR A D60 AT12 SA\_DQ[60]  
DDR A D61 AL13 SA\_DQ[61]  
DDR A D62 AR14 SA\_DQ[62]  
DDR A D63 AP14 SA\_DQ[63]

10 DDR\_A\_BS0 DDR A BS0 AC3 SA\_BS[0]  
10 DDR\_A\_BS1 DDR A BS1 AB2 SA\_BS[1]  
10 DDR\_A\_BS2 DDR A BS2 U7 SA\_BS[2]

10 DDR\_A\_CAS# DDR A CAS# AE1C SA\_CAS#  
10 DDR\_A\_RAS# DDR A RAS# AB3C SA\_RAS#  
10 DDR\_A\_WE# DDR A WE# AE9C SA\_WE#

DDR SYSTEM MEMORY - A

IC:AUB\_CFD\_rPGA,R1P0  
CONN@

SA\_CK[0] AA6 DDR A\_CLK0 10  
SA\_CK#0 AA7 DDR A\_CLK0# 10  
SA\_CKE[0] P7 DDR A\_CKE0 10

SA\_CK[1] Y6 DDR A\_CLK1 10  
SA\_CK#1 Y5 DDR A\_CLK1# 10  
SA\_CKE[1] P6 DDR A\_CKE1 10

SA\_CS#0 AE2 DDR A\_CS0# 10  
SA\_CS#1 AE8 DDR A\_CS1# 10

SA\_ODT[0] AD8 DDR A\_ODT0 10  
SA\_ODT[1] AF9 DDR A\_ODT1 10

SA\_DM[0] B9 DDR A\_DM0  
SA\_DM[1] D7 DDR A\_DM1  
SA\_DM[2] L7 DDR A\_DM2  
SA\_DM[3] M7 DDR A\_DM3  
SA\_DM[4] AG6 DDR A\_DM4  
SA\_DM[5] AM7 DDR A\_DM5  
SA\_DM[6] AN10 DDR A\_DM6  
SA\_DM[7] AN13 DDR A\_DM7

SA\_DQS#0 C9 DDR A\_DQS#0  
SA\_DQS#1 C8 DDR A\_DQS#1  
SA\_DQS#2 C8 DDR A\_DQS#2  
SA\_DQS#3 C9 DDR A\_DQS#3  
SA\_DQS#4 AH7 DDR A\_DQS#4  
SA\_DQS#5 AK9 DDR A\_DQS#5  
SA\_DQS#6 AP11 DDR A\_DQS#6  
SA\_DQS#7 AT13 DDR A\_DQS#7

SA\_DQS[0] C8 DDR A\_DQS0  
SA\_DQS[1] F9 DDR A\_DQS1  
SA\_DQS[2] L9 DDR A\_DQS2  
SA\_DQS[3] M9 DDR A\_DQS3  
SA\_DQS[4] AH8 DDR A\_DQS4  
SA\_DQS[5] AK10 DDR A\_DQS5  
SA\_DQS[6] AN11 DDR A\_DQS6  
SA\_DQS[7] AR13 DDR A\_DQS7

SA\_MA[0] Y3 DDR A\_MA0  
SA\_MA[1] W1 DDR A\_MA1  
SA\_MA[2] AA8 DDR A\_MA2  
SA\_MA[3] AA3 DDR A\_MA3  
SA\_MA[4] V1 DDR A\_MA4  
SA\_MA[5] AA9 DDR A\_MA5  
SA\_MA[6] V8 DDR A\_MA6  
SA\_MA[7] T1 DDR A\_MA7  
SA\_MA[8] Y9 DDR A\_MA8  
SA\_MA[9] U6 DDR A\_MA9  
SA\_MA[10] AD4 DDR A\_MA10  
SA\_MA[11] U3 DDR A\_MA12  
SA\_MA[12] AG8 DDR A\_MA13  
SA\_MA[13] T3 DDR A\_MA14  
SA\_MA[14] V9 DDR A\_MA15

11 DDR\_B\_D[0..63]  
11 DDR\_B\_DM[0..7]  
11 DDR\_B\_DQS[0..7]  
11 DDR\_B\_MA[0..15]

JCPU1D

DDR B D0 B5 SB\_DQ[0]  
DDR B D1 A5 SB\_DQ[1]  
DDR B D2 C3 SB\_DQ[2]  
DDR B D3 B3 SB\_DQ[3]  
DDR B D4 E4 SB\_DQ[4]  
DDR B D5 A6 SB\_DQ[5]  
DDR B D6 C4 SB\_DQ[6]  
DDR B D7 D1 SB\_DQ[7]  
DDR B D8 D1 SB\_DQ[8]  
DDR B D9 D2 SB\_DQ[9]  
DDR B D10 F2 SB\_DQ[10]  
DDR B D11 F1 SB\_DQ[11]  
DDR B D12 C2 SB\_DQ[12]  
DDR B D13 F5 SB\_DQ[13]  
DDR B D14 F3 SB\_DQ[14]  
DDR B D15 G4 SB\_DQ[15]  
DDR B D16 H6 SB\_DQ[16]  
DDR B D17 G2 SB\_DQ[17]  
DDR B D18 J6 SB\_DQ[18]  
DDR B D19 J3 SB\_DQ[19]  
DDR B D20 G5 SB\_DQ[20]  
DDR B D21 J2 SB\_DQ[21]  
DDR B D22 J1 SB\_DQ[22]  
DDR B D23 J5 SB\_DQ[23]  
DDR B D24 K2 SB\_DQ[24]  
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DDR B D26 M1 SB\_DQ[26]  
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DDR B D29 K5 SB\_DQ[29]  
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DDR B D37 AG3 SB\_DQ[37]  
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DDR B D39 AH4 SB\_DQ[39]  
DDR B D40 AK4 SB\_DQ[40]  
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DDR B D44 AK5 SB\_DQ[44]  
DDR B D45 AK2 SB\_DQ[45]  
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DDR B D47 AM3 SB\_DQ[47]  
DDR B D48 AP3 SB\_DQ[48]  
DDR B D49 AN5 SB\_DQ[49]  
DDR B D50 AT4 SB\_DQ[50]  
DDR B D51 AN6 SB\_DQ[51]  
DDR B D52 AN4 SB\_DQ[52]  
DDR B D53 AN5 SB\_DQ[53]  
DDR B D54 AT5 SB\_DQ[54]  
DDR B D55 AT6 SB\_DQ[55]  
DDR B D56 AN7 SB\_DQ[56]  
DDR B D57 AP6 SB\_DQ[57]  
DDR B D58 AP8 SB\_DQ[58]  
DDR B D59 AT9 SB\_DQ[59]  
DDR B D60 AT7 SB\_DQ[60]  
DDR B D61 AP9 SB\_DQ[61]  
DDR B D62 AR10 SB\_DQ[62]  
DDR B D63 AT10 SB\_DQ[63]

11 DDR\_B\_BS0 DDR B\_BS0 AB1 SB\_BS[0]  
11 DDR\_B\_BS1 DDR B\_BS1 W5 SB\_BS[1]  
11 DDR\_B\_BS2 DDR B\_BS2 R7 SB\_BS[2]

11 DDR\_B\_CAS# DDR B\_CAS# AC5C SB\_CAS#  
11 DDR\_B\_RAS# DDR B\_RAS# Y7C SB\_RAS#  
11 DDR\_B\_WE# DDR B\_WE# AC6C SB\_WE#

SB\_CK[0] W8 DDR B\_CLK0 11  
SB\_CK#0 W9 DDR B\_CLK0# 11  
SB\_CKE[0] M3 DDR B\_CKE0 11

SB\_CK[1] V7 DDR B\_CLK1 11  
SB\_CK#1 V6 DDR B\_CLK1# 11  
SB\_CKE[1] M2 DDR B\_CKE1 11

SB\_CS#0 AB8 DDR B\_CS0# 11  
SB\_CS#1 AD6 DDR B\_CS1# 11

SB\_ODT[0] AC7 DDR B\_ODT0 11  
SB\_ODT[1] AD1 DDR B\_ODT1 11

SB\_DM[0] D4 DDR B\_DM0  
SB\_DM[1] E1 DDR B\_DM1  
SB\_DM[2] H3 DDR B\_DM2  
SB\_DM[3] K1 DDR B\_DM3  
SB\_DM[4] AH1 DDR B\_DM4  
SB\_DM[5] AL2 DDR B\_DM5  
SB\_DM[6] AR4 DDR B\_DM6  
SB\_DM[7] AT8 DDR B\_DM7

SB\_DQS#0 D5 DDR B\_DQS#0  
SB\_DQS#1 E4 DDR B\_DQS#1  
SB\_DQS#2 D4 DDR B\_DQS#2  
SB\_DQS#3 L4 DDR B\_DQS#3  
SB\_DQS#4 AH2 DDR B\_DQS#4  
SB\_DQS#5 AL4 DDR B\_DQS#5  
SB\_DQS#6 AR5 DDR B\_DQS#6  
SB\_DQS#7 AR8 DDR B\_DQS#7

SB\_DQS[0] C5 DDR B\_DQS0  
SB\_DQS[1] E3 DDR B\_DQS1  
SB\_DQS[2] H4 DDR B\_DQS2  
SB\_DQS[3] M5 DDR B\_DQS3  
SB\_DQS[4] AG2 DDR B\_DQS4  
SB\_DQS[5] AL5 DDR B\_DQS5  
SB\_DQS[6] AP5 DDR B\_DQS6  
SB\_DQS[7] AR7 DDR B\_DQS7

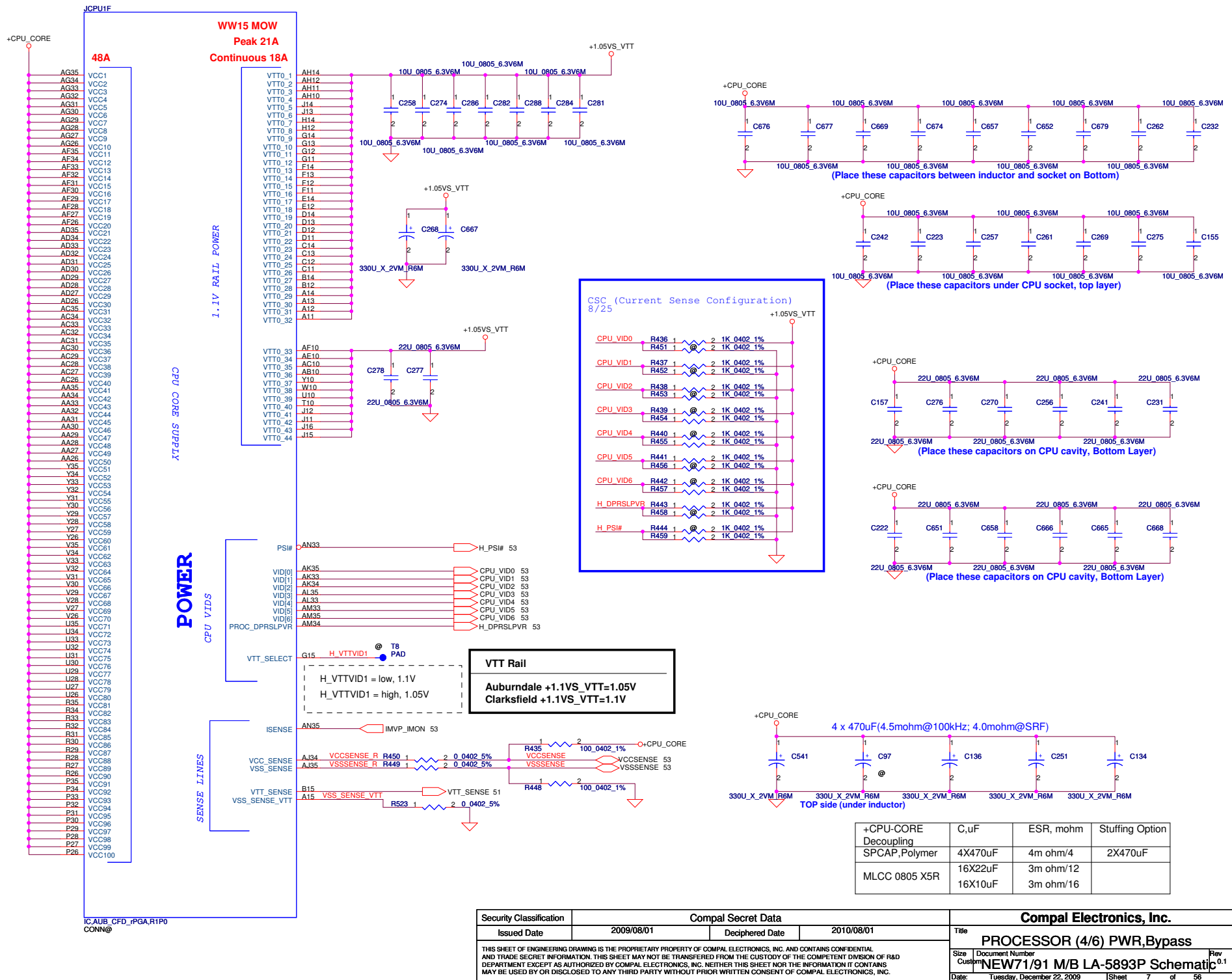
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SB\_MA[1] V2 DDR B\_MA1  
SB\_MA[2] T5 DDR B\_MA2  
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SB\_MA[4] B1 DDR B\_MA4  
SB\_MA[5] T8 DDR B\_MA5  
SB\_MA[6] R2 DDR B\_MA6  
SB\_MA[7] R6 DDR B\_MA7  
SB\_MA[8] B4 DDR B\_MA8  
SB\_MA[9] R5 DDR B\_MA9  
SB\_MA[10] AB5 DDR B\_MA10  
SB\_MA[11] P3 DDR B\_MA11  
SB\_MA[12] R3 DDR B\_MA12  
SB\_MA[13] AF7 DDR B\_MA13  
SB\_MA[14] P5 DDR B\_MA14  
SB\_MA[15] N1 DDR B\_MA15

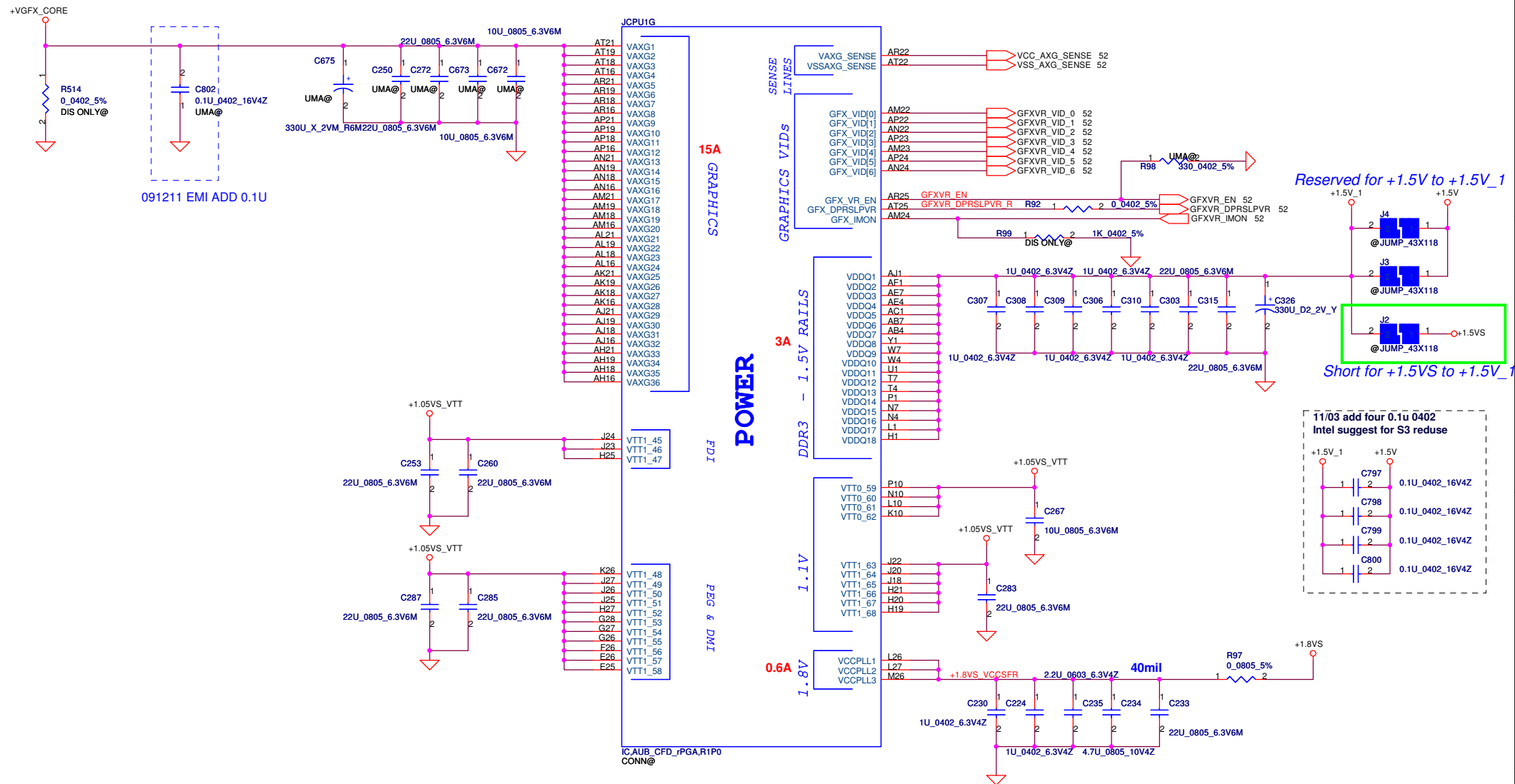
DDR SYSTEM MEMORY - B

IC:AUB\_CFD\_rPGA,R1P0  
CONN@

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								PROCESSOR (3/6) DDRIII					
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						Date		Tuesday, December 22, 2009		Sheet		6 of 56	

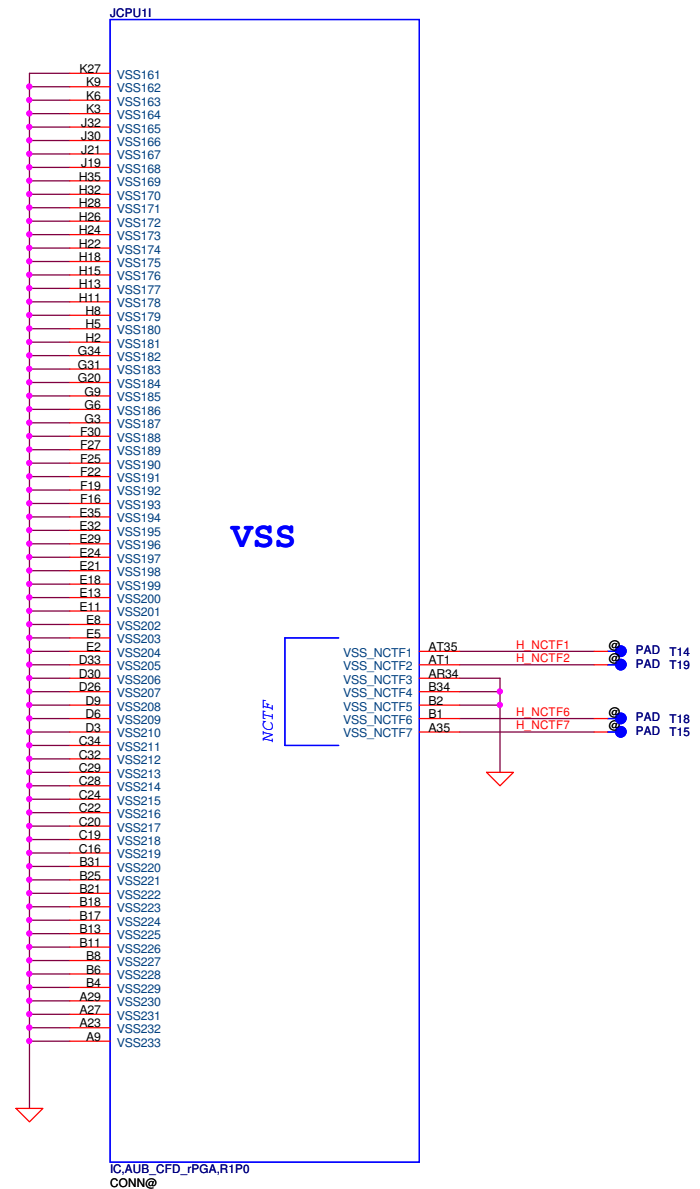
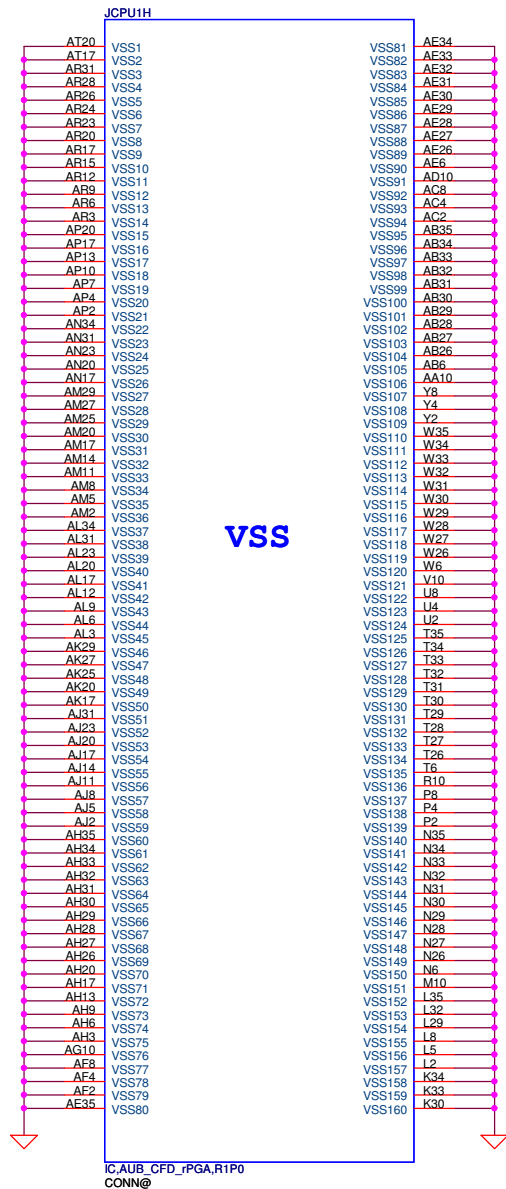




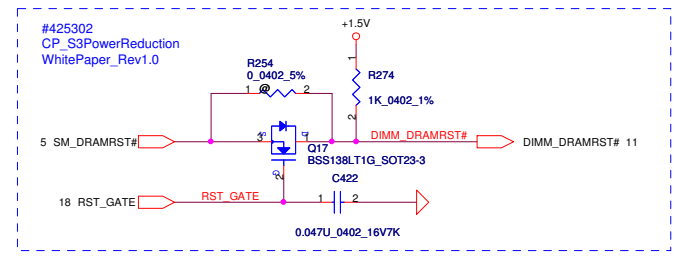
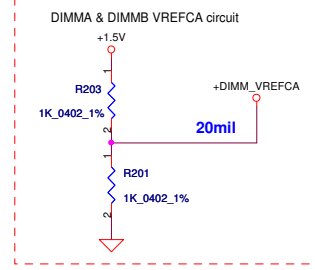
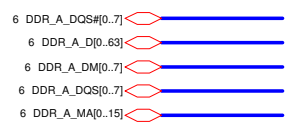
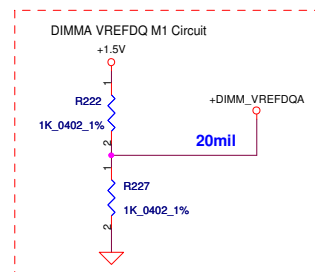


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Size		Document Number		Rev	
Customer		NEW71/91 M/B LA-5893P Schematic		0.1	
Date		Tuesday, December 22, 2009		Sheet 8 of 56	

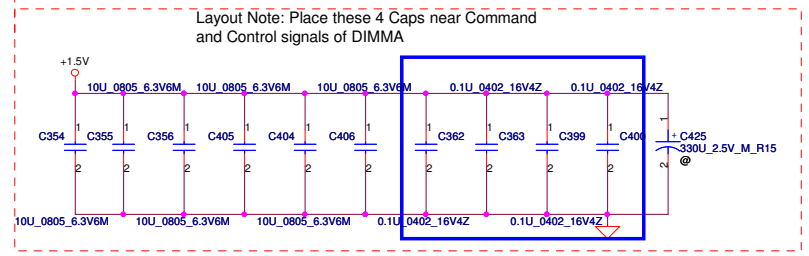




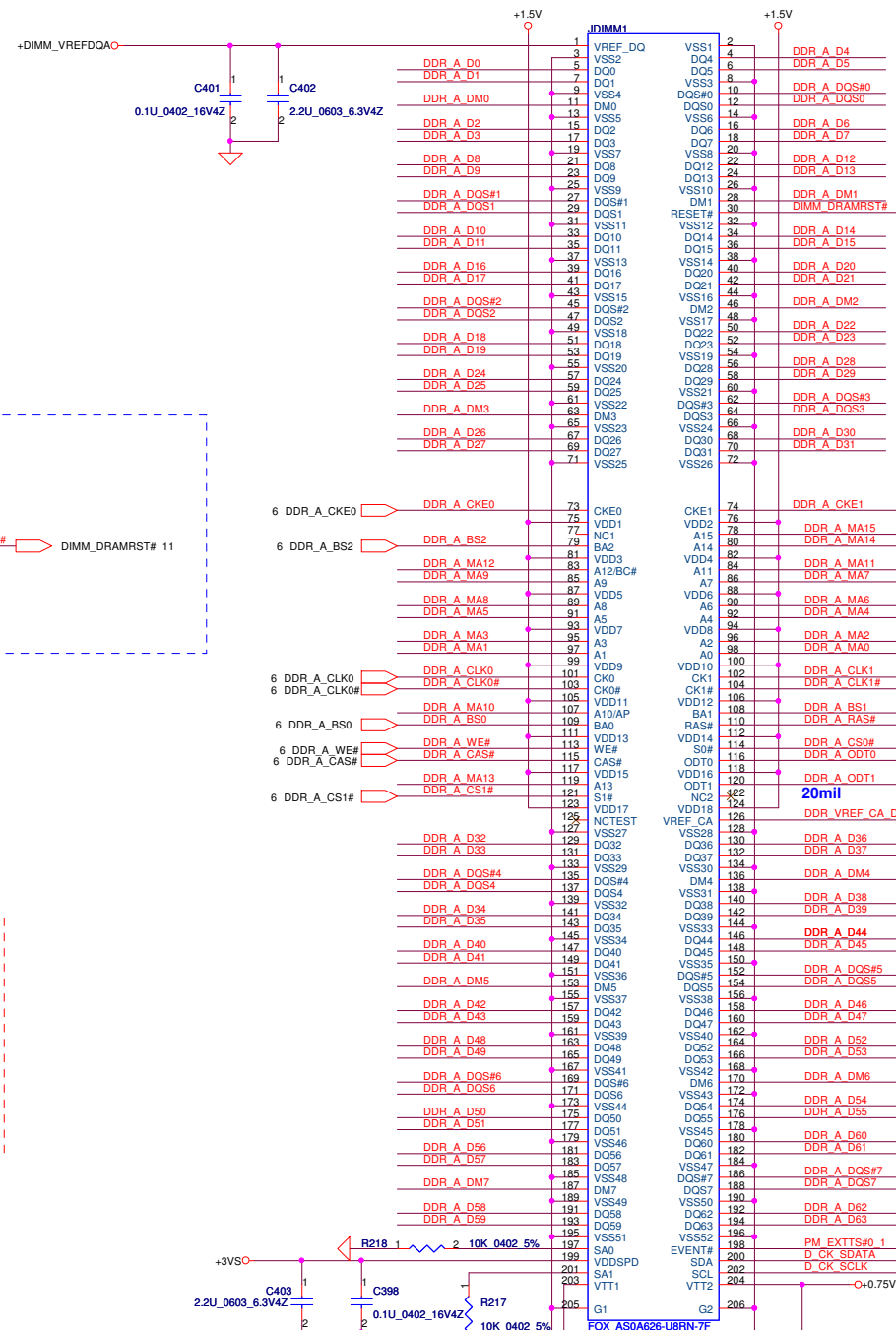
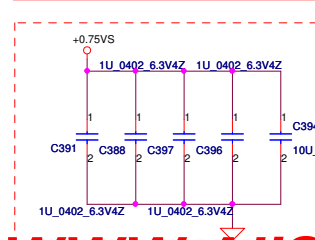
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								Size	Document Number		Rev
								Customer	NEW71/91 M/B LA-5893P Schematic		0.1
								Date:	Friday, December 18, 2009	Sheet	9



**Layout Note:**  
Place near JDIMM1



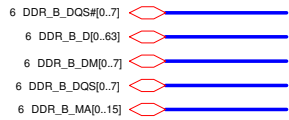
**Layout Note:**  
Place near JDIMM1.203 & JDIMM1.204



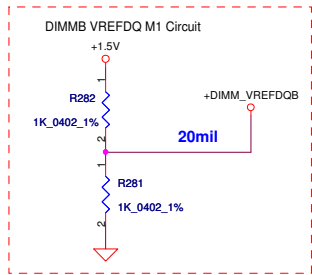
**DDR3 SO-DIMM A**  
**H=8mm**

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				Date: Tuesday, December 22, 2009				Rev 0.1			
				1				10 of 56			

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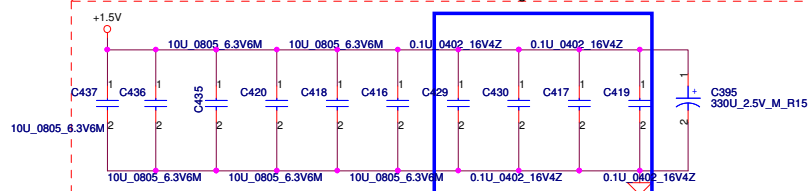


2008/9/8 #400755  
Calpella Clarkfield  
DDR3 SO-DIMM  
VREFDQ Platform  
Design Guide Change Details

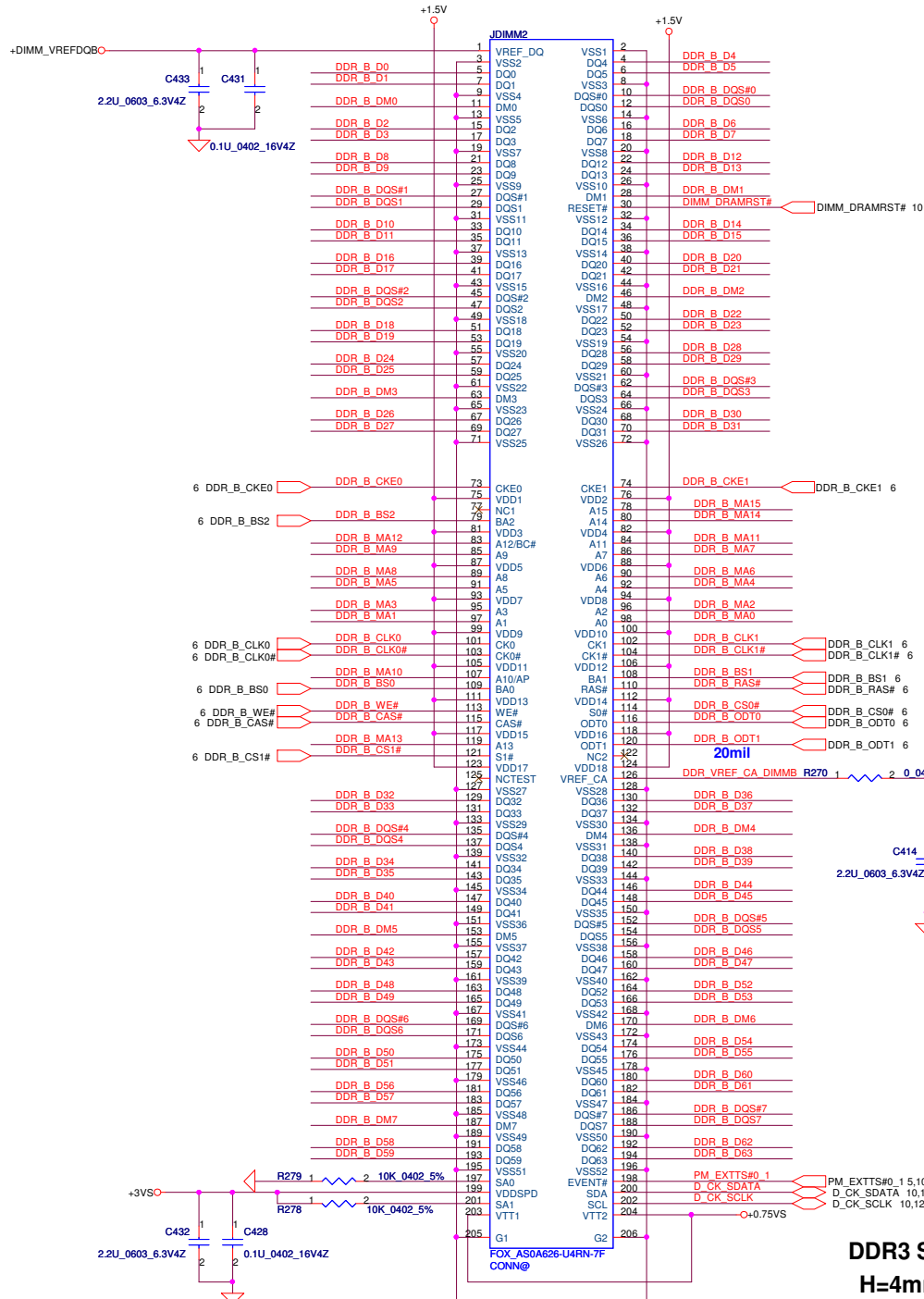
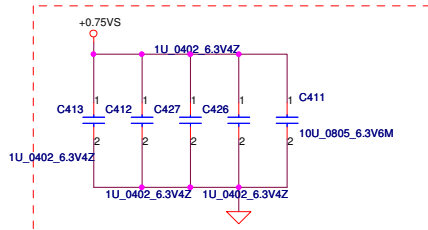


Layout Note:  
Place near JDIMM2

Layout Note: Place these 4 Caps near Command  
and Control signals of DIMMB



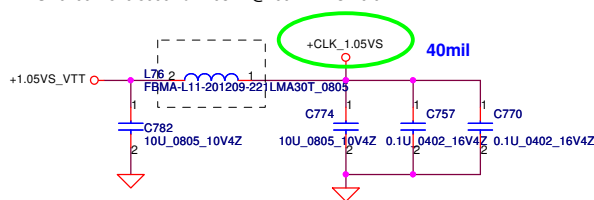
Layout Note:  
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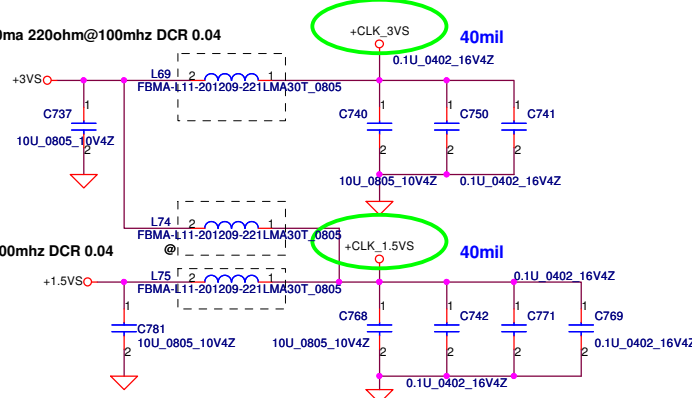
DDR3 SO-DIMM B  
H=4mm

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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	
				DDRIII-SODIMM SLOT2	
				Size   Document Number	Rev
				Customer	NEW71/91 M/B LA-5893P Schematic 0.1
				Date	Tuesday, December 22, 2009
				Sheet	11 of 56

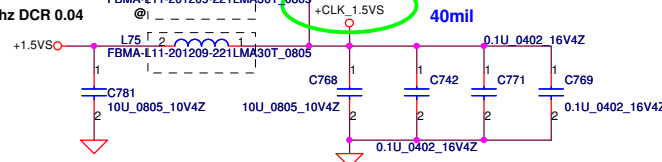
SM010014520 3000ma 220ohm@100mhz DCR 0.04



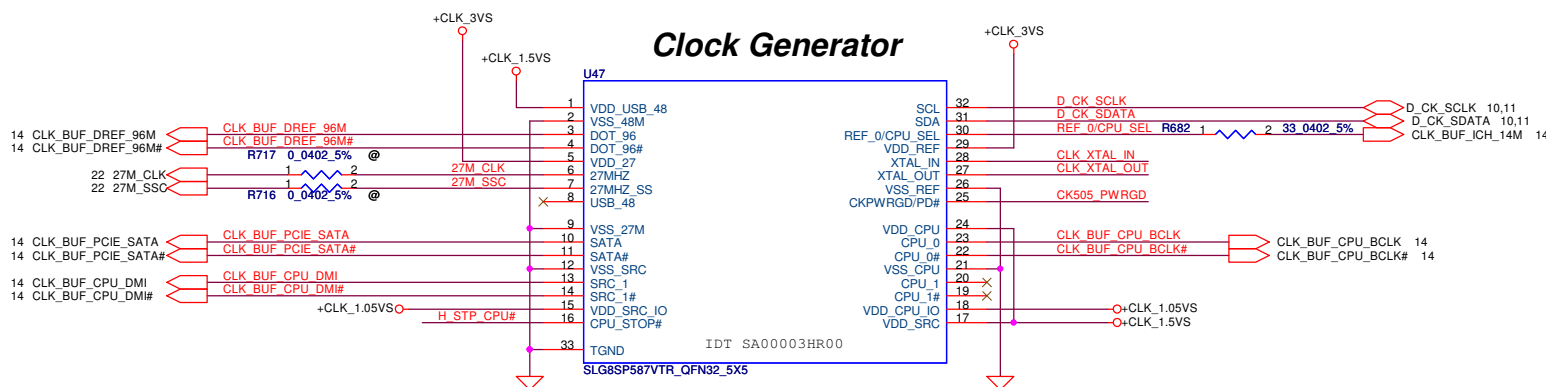
SM010014520 3000ma 220ohm@100mhz DCR 0.04



SM010014520 3000ma 220ohm@100mhz DCR 0.04

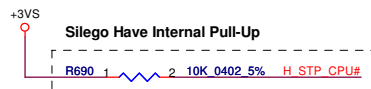


## Clock Generator

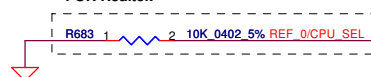


IDT: 9LRS3199AKLFT, SA000030P00  
SILEGO: SLG8SP587V(WF), SA00002XY10  
Low Power:  
IDT: 9LVS3199AKLFT, SA00003HR00  
Realtek: RTM890N-631-VB-GRT, SA00003HQ10

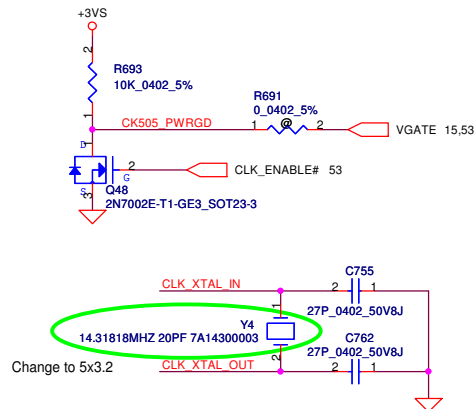
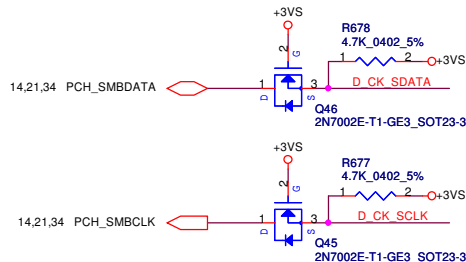
IDT 9LVS3199AKLFT NC



IDT Have Internal Pull-Down  
FOR Realtek



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

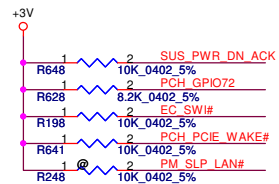
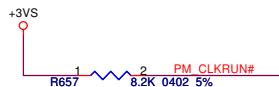
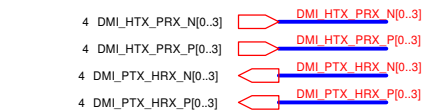


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								Size		Document Number		Customer	
								NEW71/91		M/B LA-5893P Schematic		0.1	
								Tuesday, December 22, 2009		12		of 56	



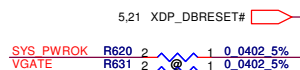






+1.05VS\_PCH

09/09/14 WW37 PCH WAKE# PU 10K

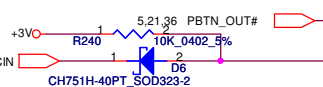


LAN\_RST#

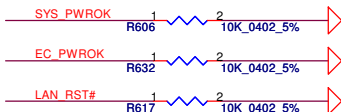
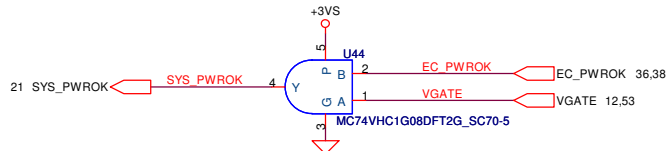
5 PM\_DRAM\_PWRGD

PCH\_RSMRST#

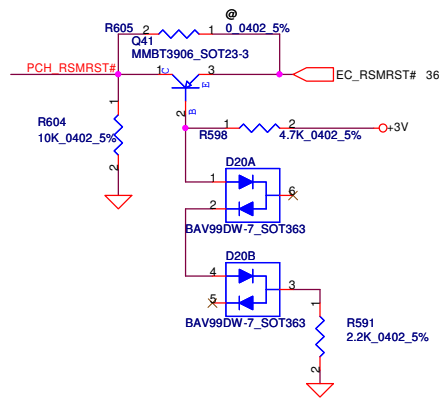
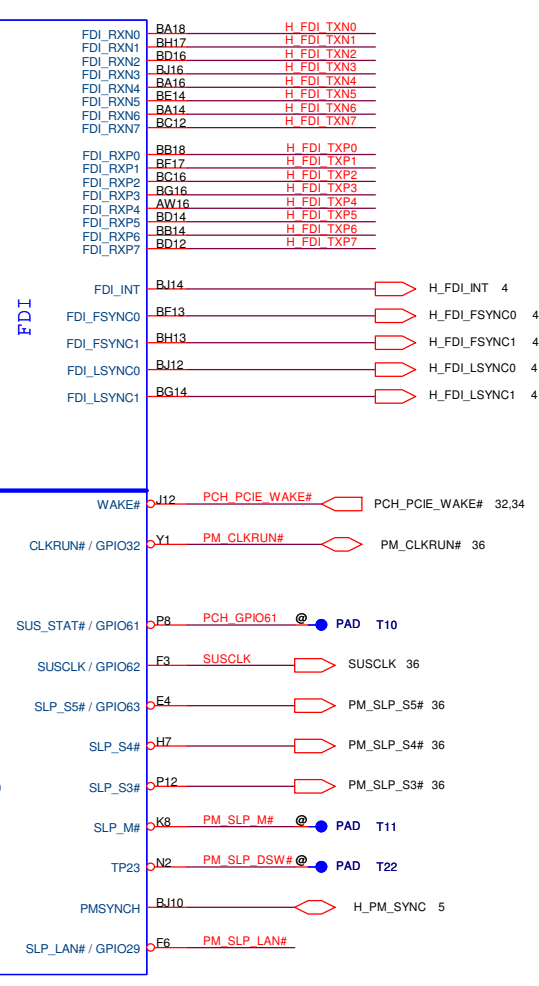
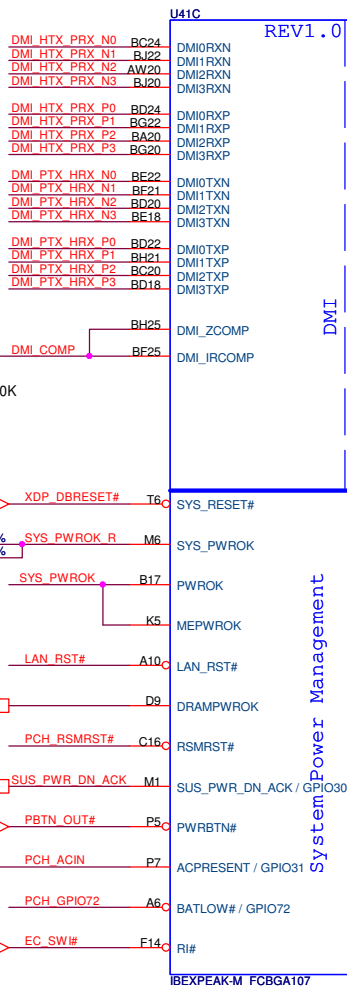
36 SUS\_PWR\_DN\_ACK



36 EC\_SWI#

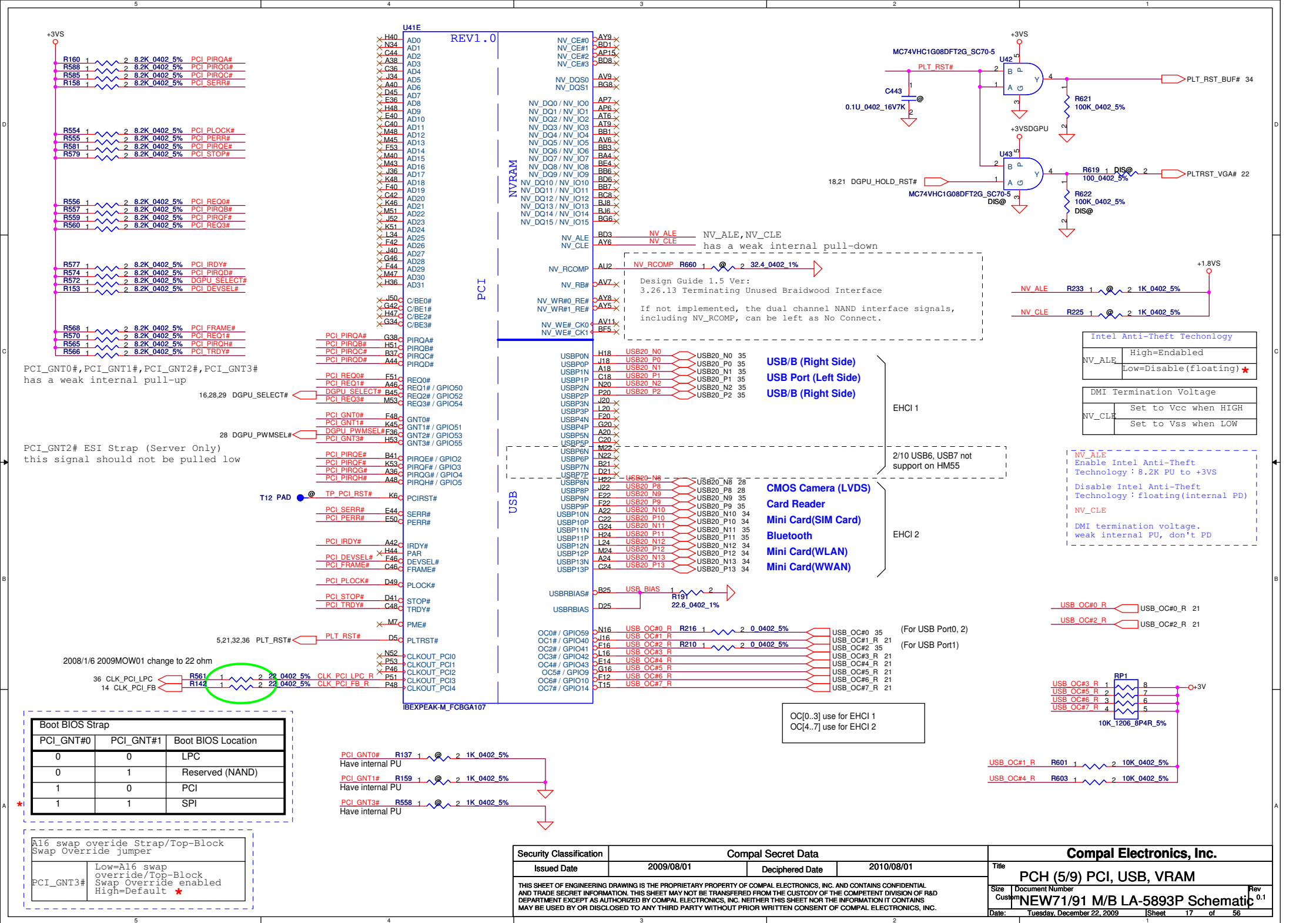


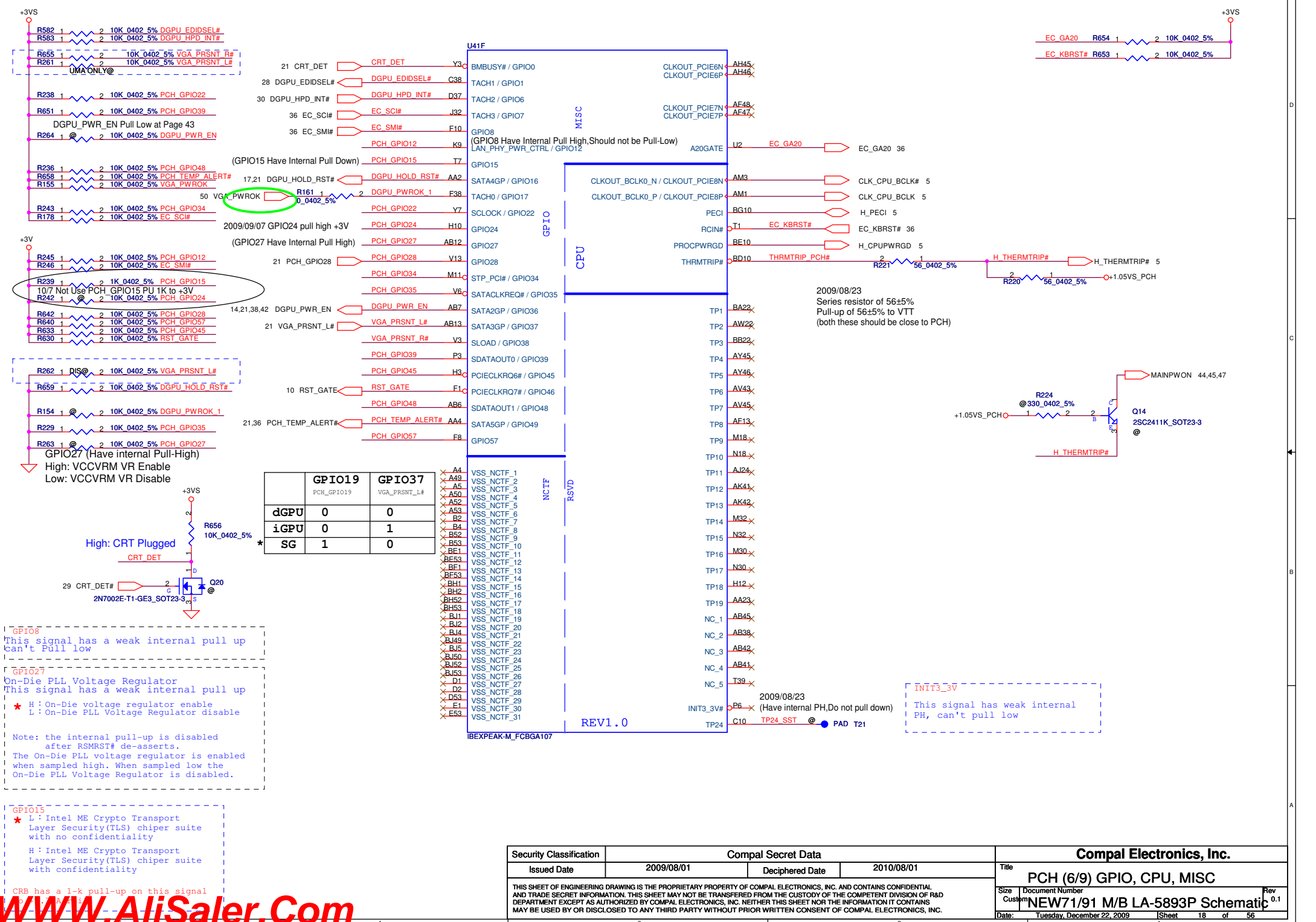
No used Integrated LAN,  
connecting LAN\_RST# to GND

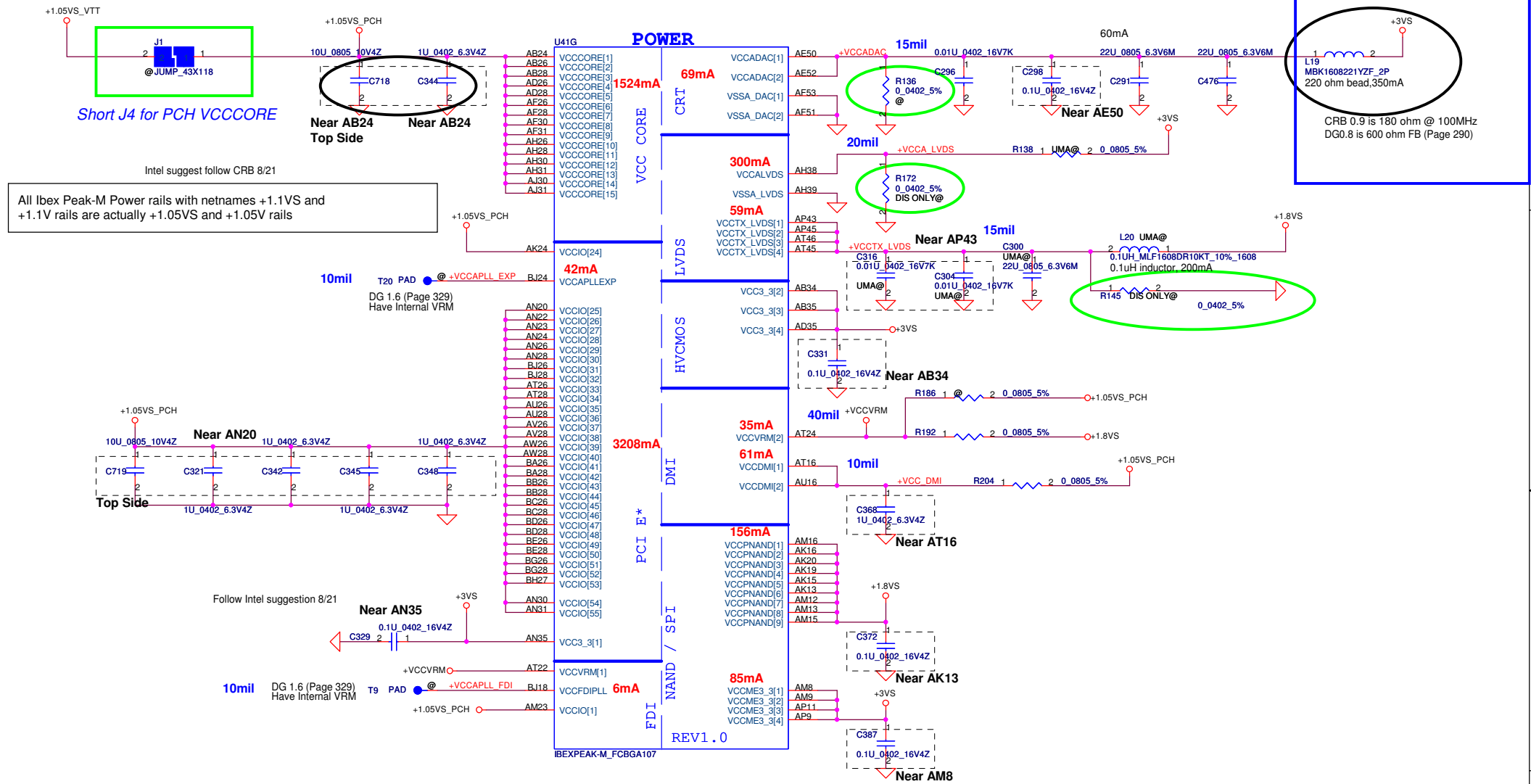


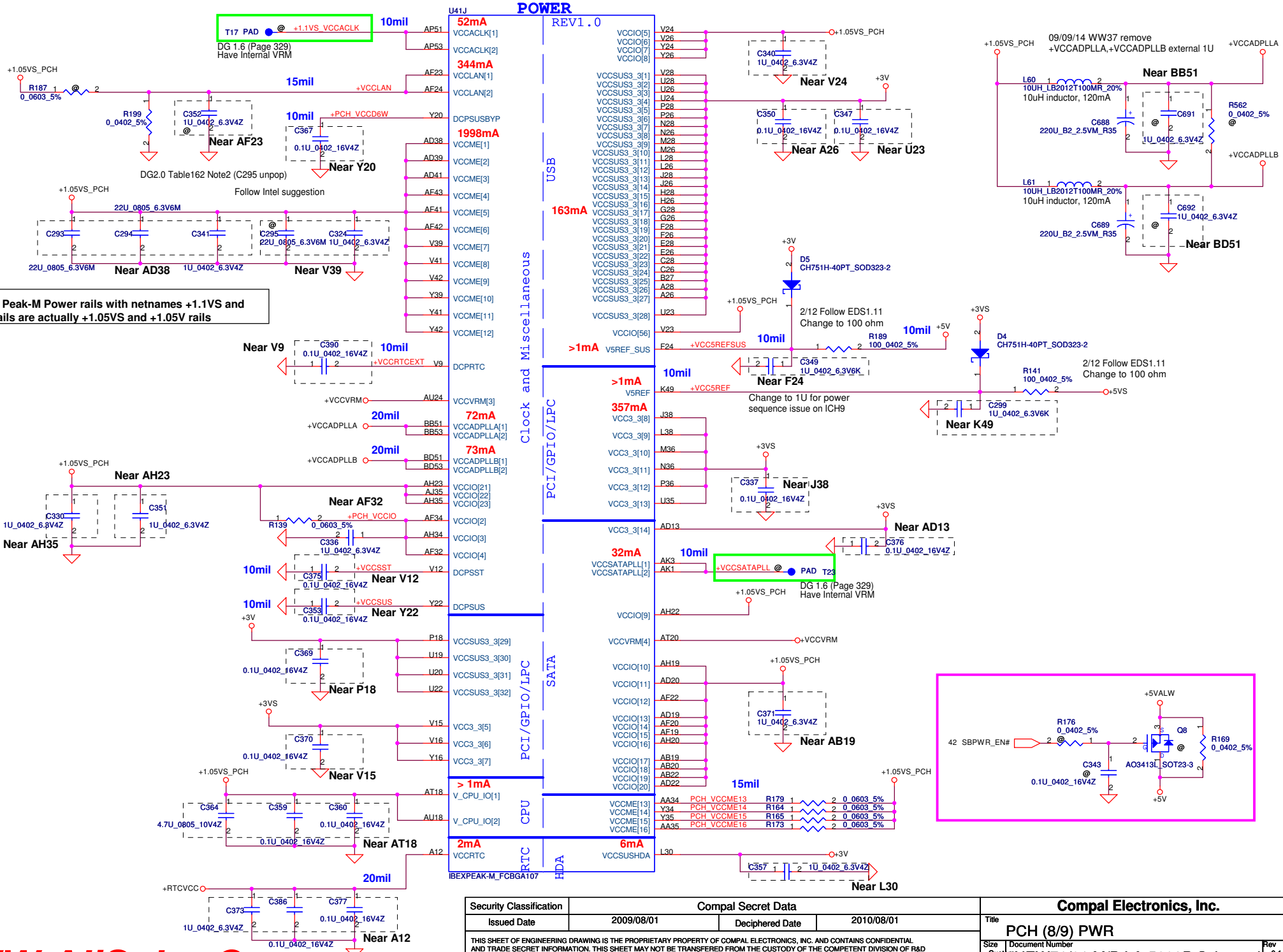
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				Date	Tuesday, December 22, 2009
				Sheet	15 of 56
				Rev	0.1







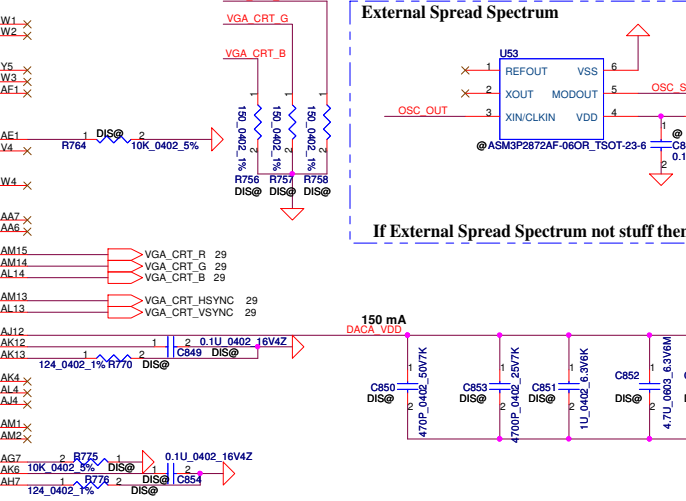
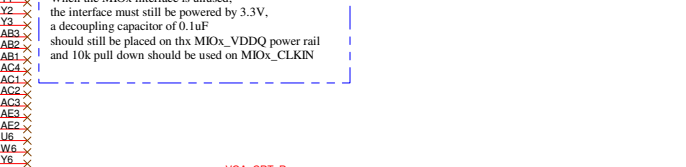
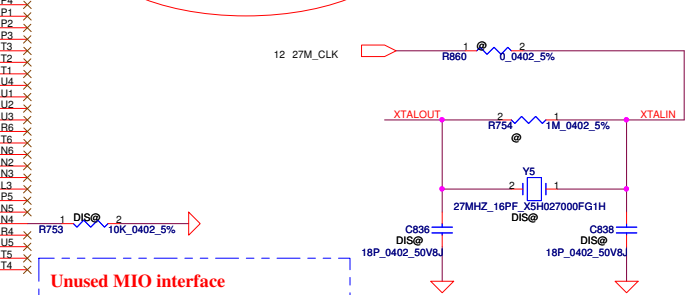
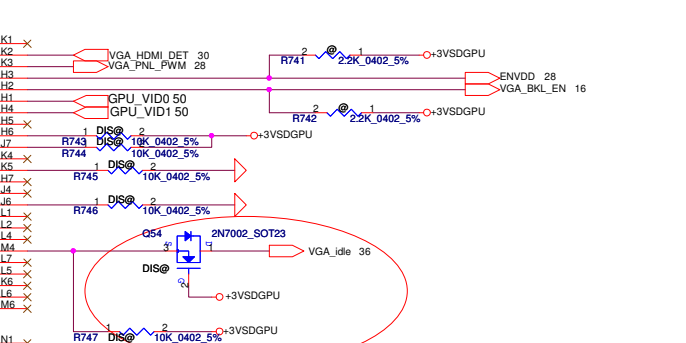
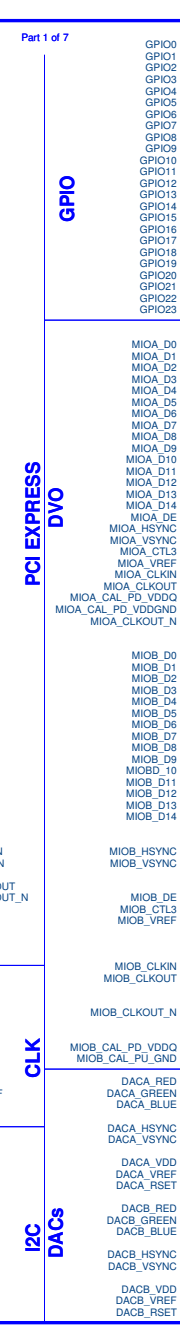
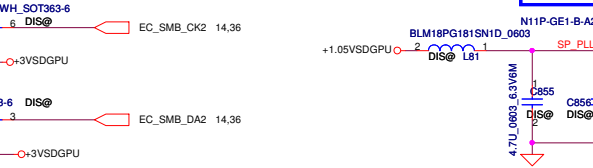
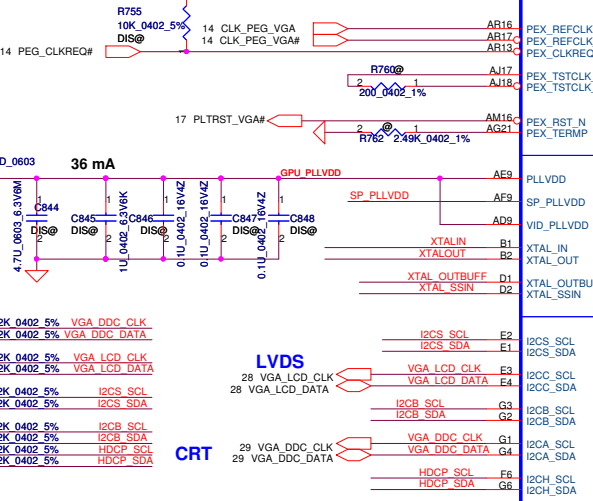
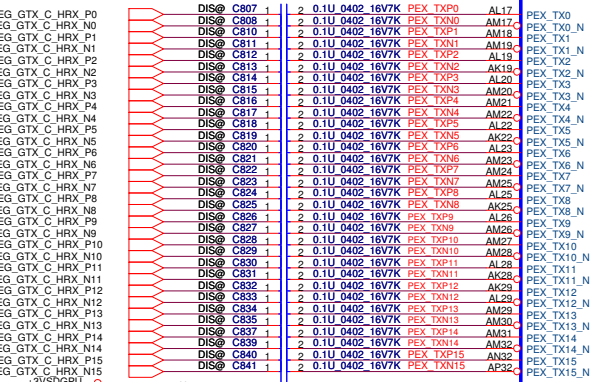
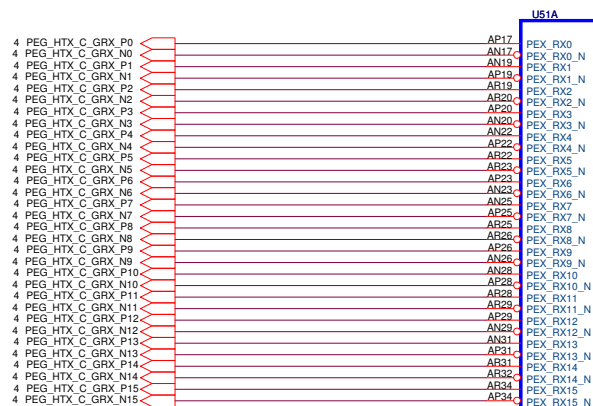




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				Date	Tuesday, December 22, 2009
				Sheet	20 of 56

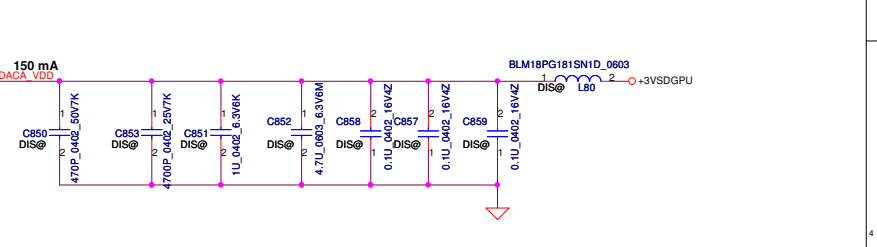
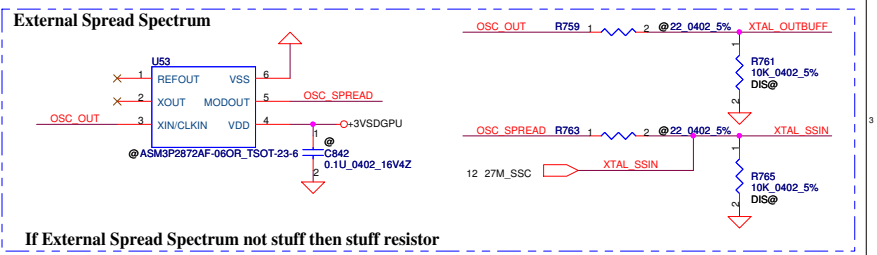






GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	N/A
GPIO8	IN	L	N/A
GPIO9	OUT	L	N/A
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A

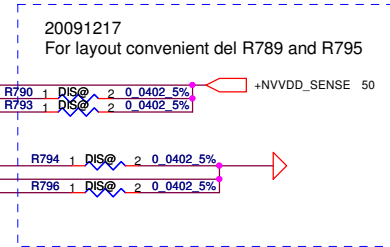
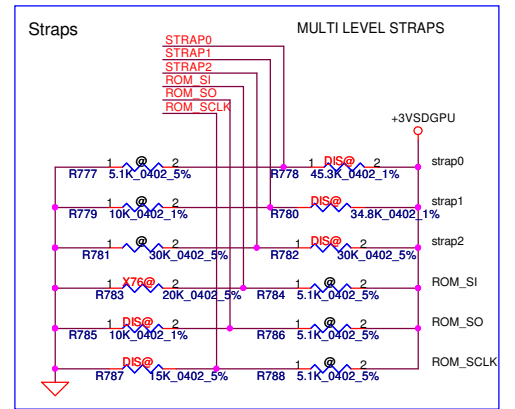
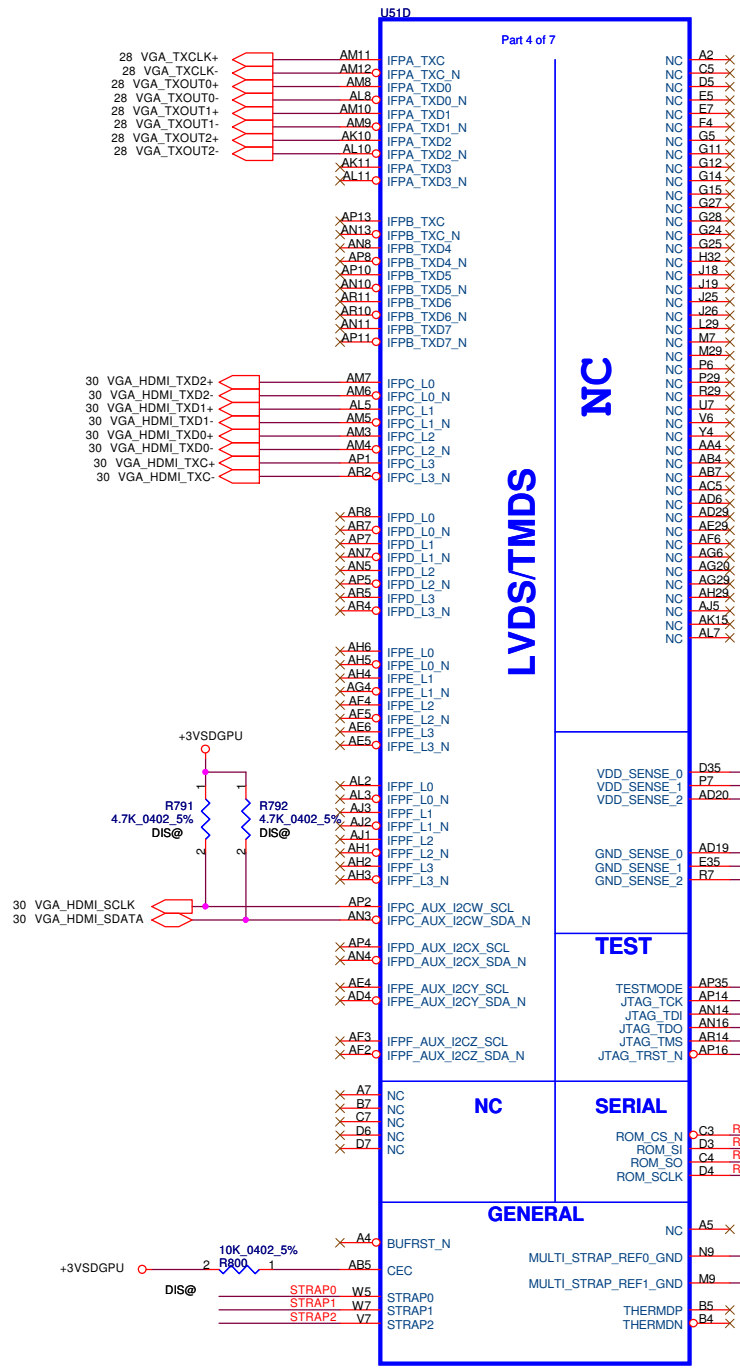
**Unused MIO interface**  
When the MIO interface is unused, the interface must still be powered by 3.3V, a decoupling capacitor of 0.1uF should still be placed on the MIOx\_VDDQ power rail and 10k pull down should be used on MIOx\_CLKIN



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Date	Wednesday, December 23, 2009	Sheet	22	of	56

Mode E Command Mapping GB2-128 Package Femi	Mode C Command Mapping GB1-128 Package		
	Data Bit	0..31	32..63
FBx_CMD3	FBx_CMD0	CKE_L	A8
FBx_CMD8	FBx_CMD1	A8	A8
FBx_CMD2	FBx_CMD2	CS0_L*	
FBx_CMD21	FBx_CMD3	A7	A6
FBx_CMD24	FBx_CMD4	A2	A1
FBx_CMD23	FBx_CMD5	A11	A9
FBx_CMD26	FBx_CMD6	A5	A4
FBx_CMD7	FBx_CMD7	A0	A12
FBx_CMD15	FBx_CMD8	CAS*	CAS*
FBx_CMD13	FBx_CMD9	BA1	A3
FBx_CMD4	FBx_CMD10	A9	A11
FBx_CMD18	FBx_CMD11		CS0_H
FBx_CMD29	FBx_CMD12	BA0	BA0
FBx_CMD27	FBx_CMD13	BA2	A15
FBx_CMD6	FBx_CMD14	A3	BA1
FBx_CMD17	FBx_CMD15		CS1_H
FBx_CMD19	FBx_CMD16		ODT_H
FBx_CMD22	FBx_CMD17	A4	A5
FBx_CMD12	FBx_CMD18	A13	A14
FBx_CMD28	FBx_CMD19	WE*	A10
FBx_CMD10	FBx_CMD20	A1	A2
FBx_CMD25	FBx_CMD21	A10	WE*
FBx_CMD9	FBx_CMD22	A12	A0
FBx_CMD1	FBx_CMD23	CS1_L*	
FBx_CMD11	FBx_CMD24	RAS*	RAS*
FBx_CMD0	FBx_CMD25	ODT_L	
FBx_CMD5	FBx_CMD26	A6	A7
FBx_CMD16	FBx_CMD27		CKE_H
FBx_CMD20	FBx_CMD28	RST	RST
FBx_CMD14	FBx_CMD29	A14	A13
FBx_CMD30	FBx_CMD30	A15	BA2
FBx_CMD31			

LOW HIGH



## TEST

## SERIAL

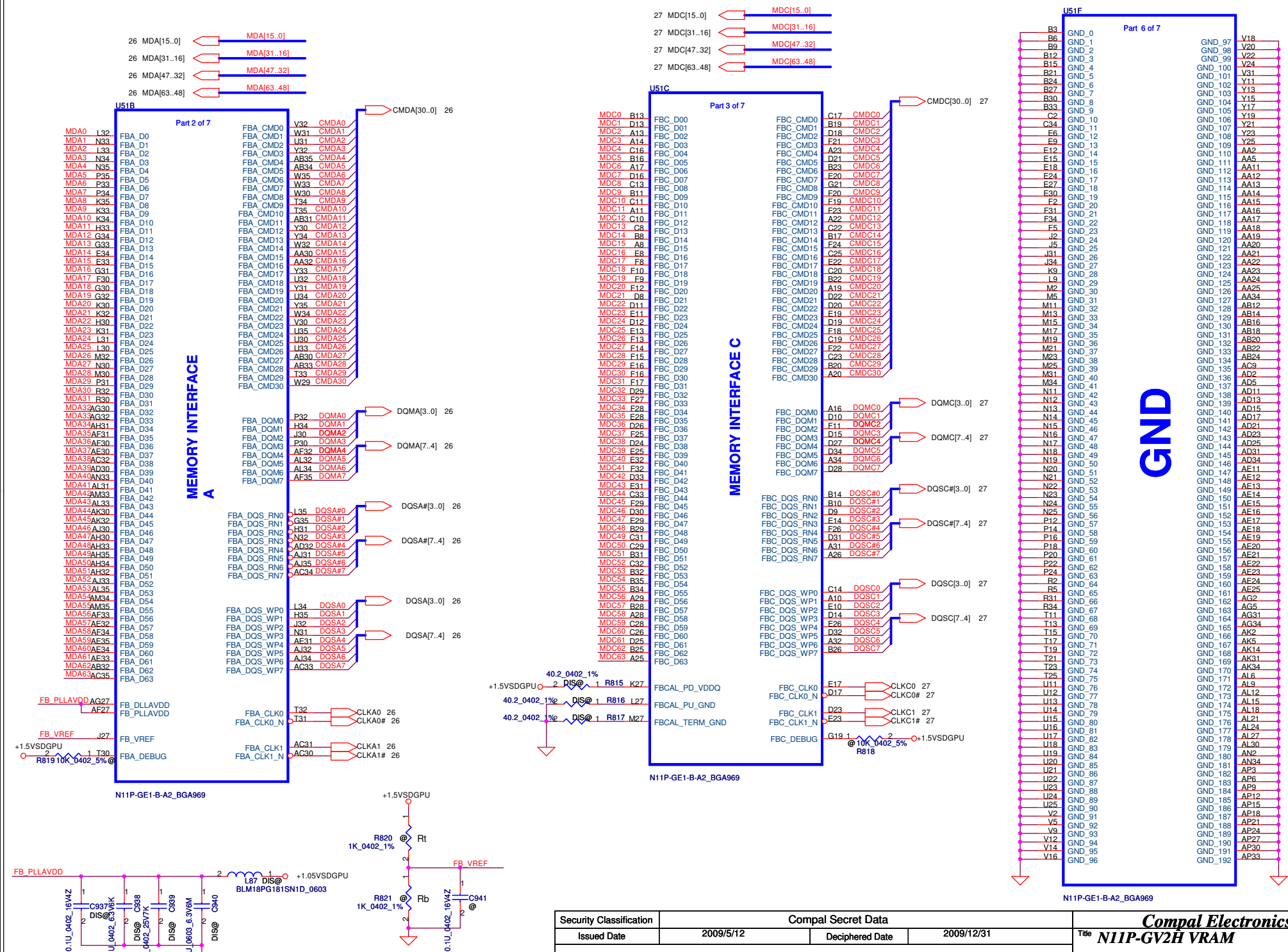
## GENERAL

N11P-GE1-B-A2\_BGA969

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				Customer	NEW71/91 M/B LA-5893P Schematic
				Date:	Tuesday, December 22, 2009
				Sheet	23 of 56







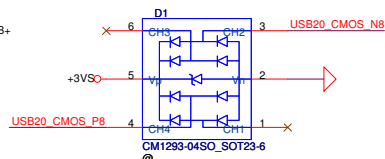
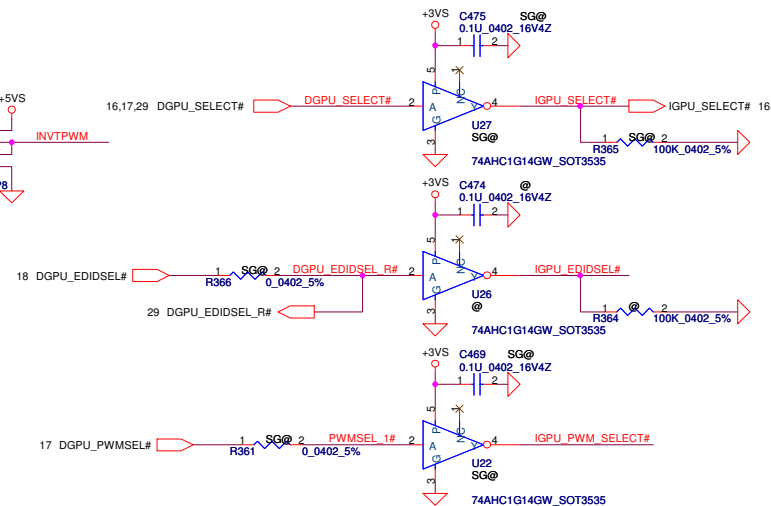
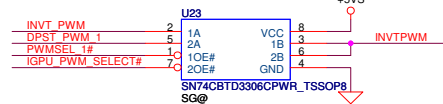
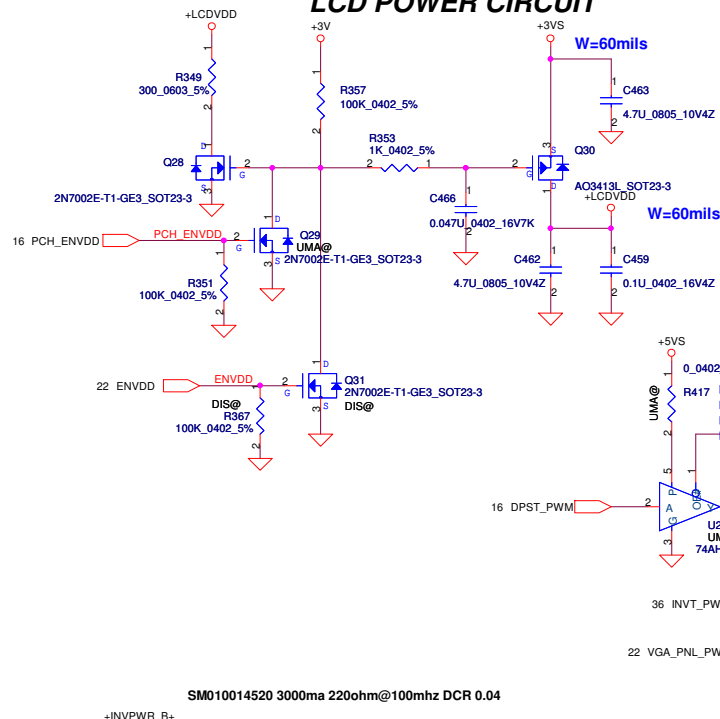
Security Classification		Compal Secret Data				<b>Compal Electronics, Inc.</b>									
Issued Date		2009/5/12		Deciphered Date		2009/12/31		Title							
								<b>N11P-GV2H VRAM</b>							
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						Customer		<b>NEW71/91 M/B LA-5893P Schematic</b>						0.1	
						Date:		Tuesday, December 22, 2009				Sheet		25 of 56	



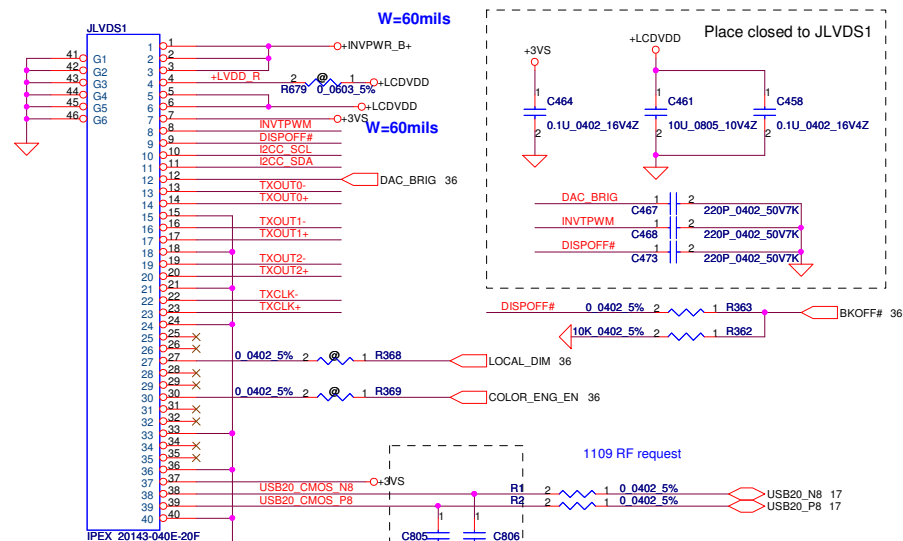




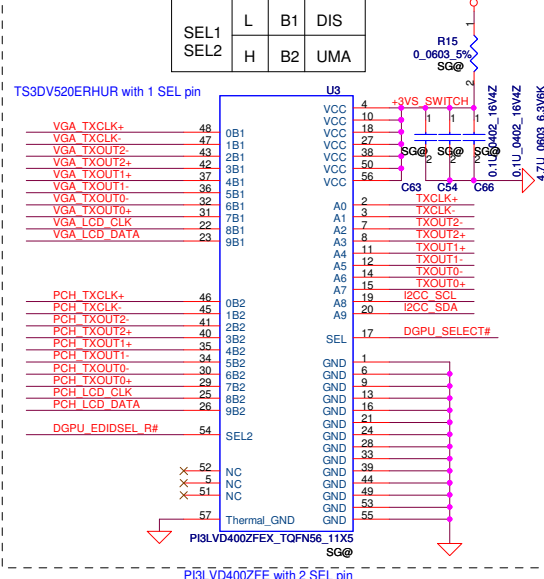
# LCD POWER CIRCUIT



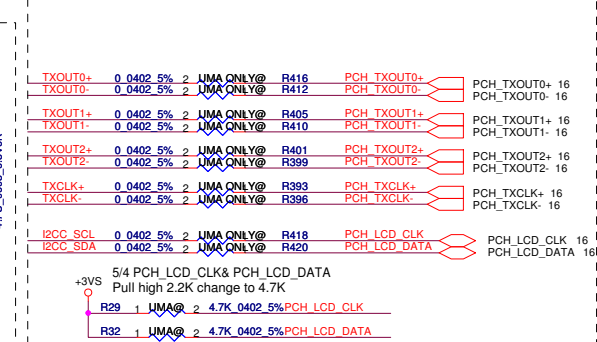
## LCD/LED PANEL Conn.



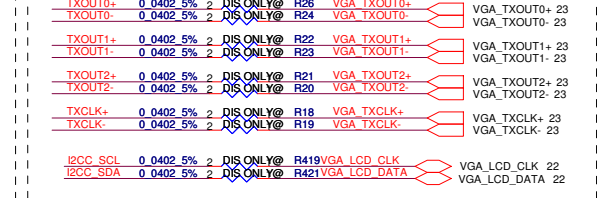
## SWITCHABLE



## UMA ONLY

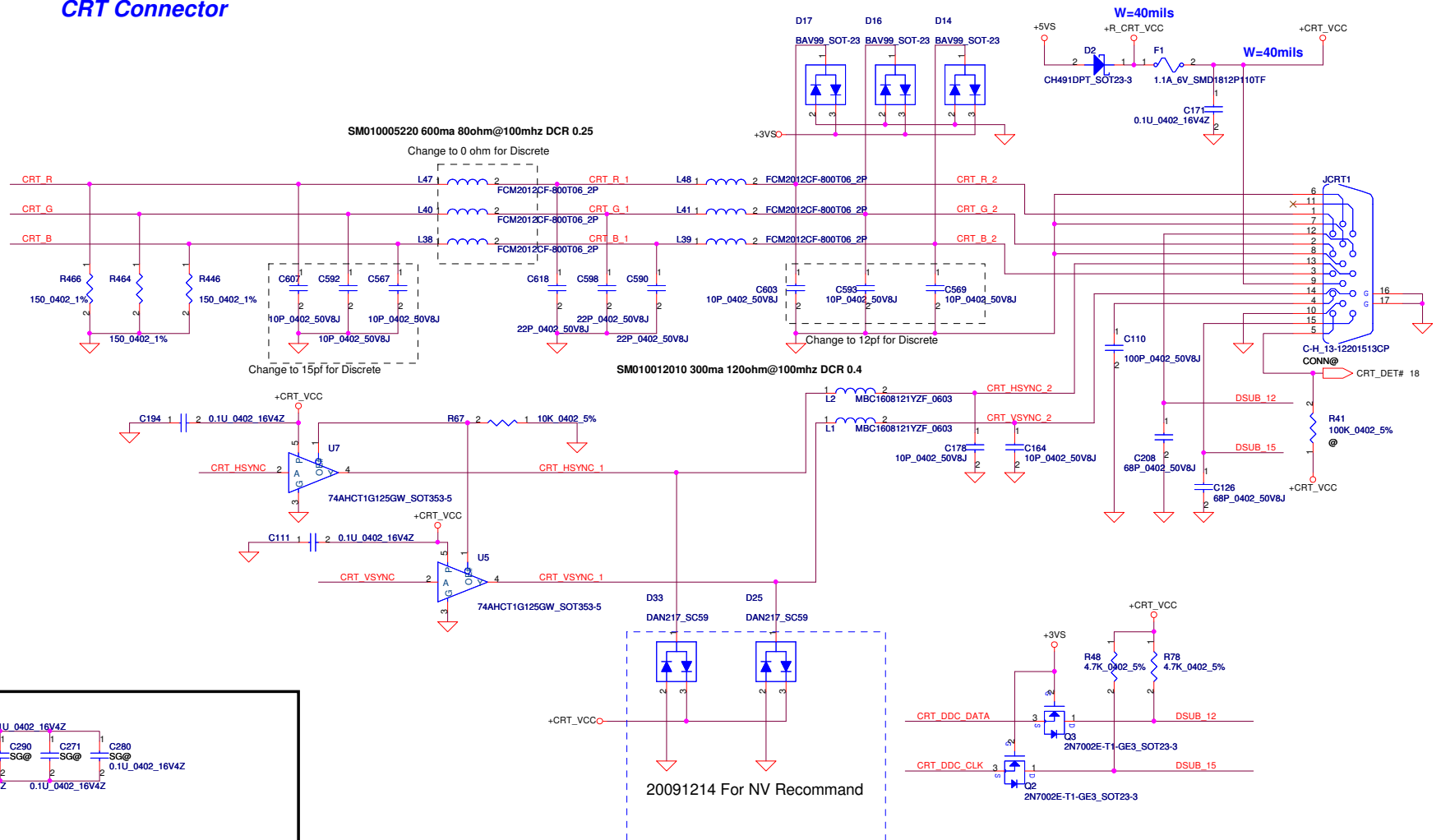


## Discrete ONLY



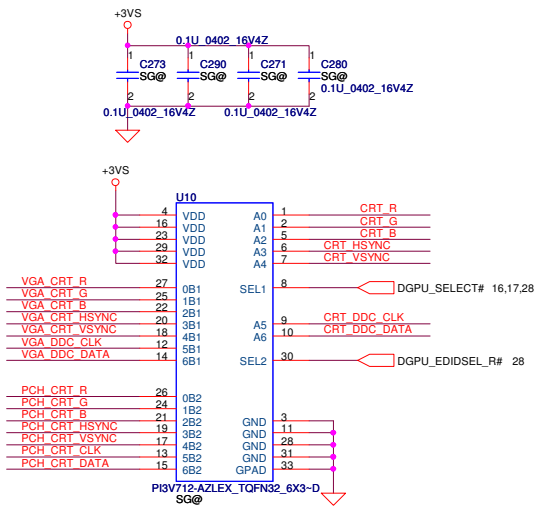
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	LVDS Connector	
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				Customer	NEW71/91 M/B LA-5893P Schematic 0.1	
				Date:	Tuesday, December 22, 2009	Sheet 28 of 56

# CRT Connector



## SWITCHABLE

2009/08/27



L	B1	DIS
H	B2	UMA

## Discrete only

22	VGA_CRT_R	VGA_CRT_R	R537	2	DIS ONLY@	0.0402_5%	CRT_R
22	VGA_CRT_G	VGA_CRT_G	R535	2	DIS ONLY@	0.0402_5%	CRT_G
22	VGA_CRT_B	VGA_CRT_B	R533	2	DIS ONLY@	0.0402_5%	CRT_B
22	VGA_CRT_HSYNC	VGA_CRT_HSYNC	R531	2	DIS ONLY@	0.0402_5%	CRT_HSYNC
22	VGA_CRT_VSYNC	VGA_CRT_VSYNC	R529	2	DIS ONLY@	0.0402_5%	CRT_VSYNC
22	VGA_DDC_CLK	VGA_DDC_CLK	R527	2	DIS ONLY@	0.0402_5%	CRT_DDC_CLK
22	VGA_DDC_DATA	VGA_DDC_DATA	R526	2	DIS ONLY@	0.0402_5%	CRT_DDC_DATA

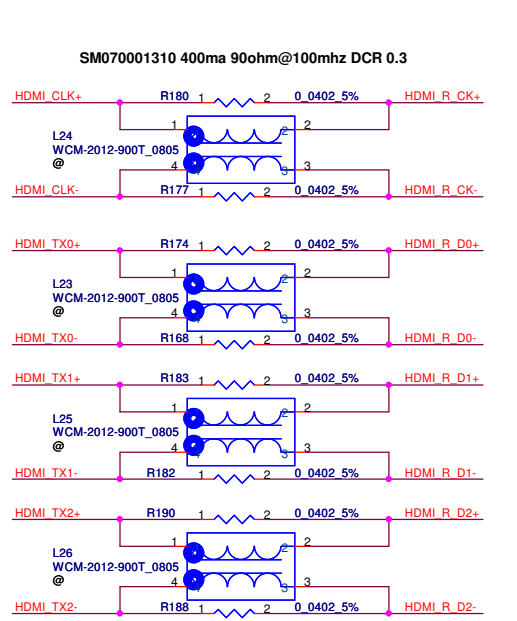
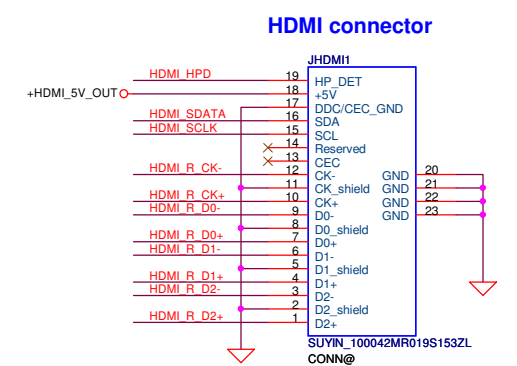
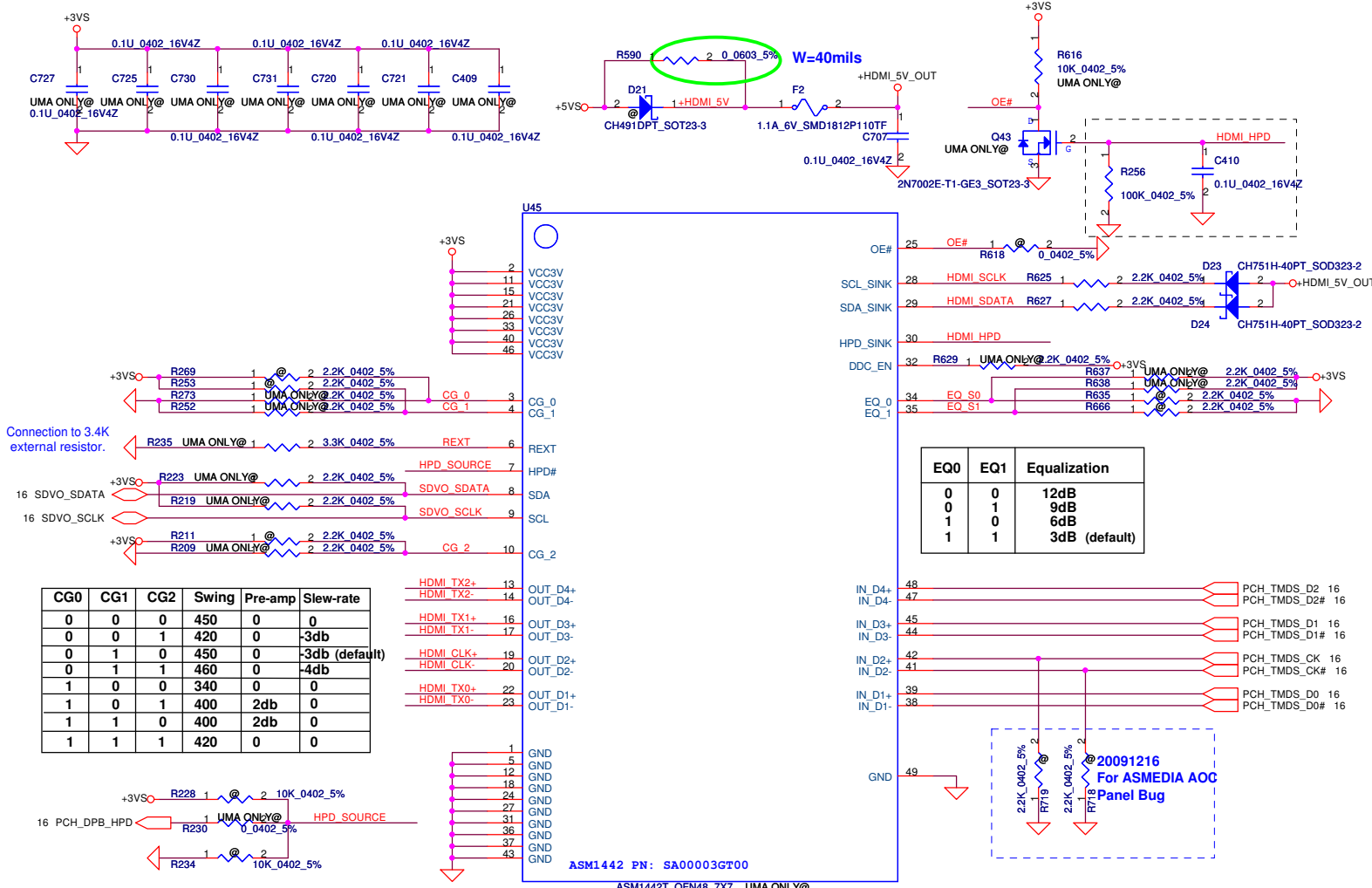
VGA\_DDC\_DATA and VGA\_DDC\_CLK Pull high at Page22

## UMA only

16	PCH_CRT_R	PCH_CRT_R	R536	2	UMA ONLY@	0.0402_5%	CRT_R
16	PCH_CRT_G	PCH_CRT_G	R534	2	UMA ONLY@	0.0402_5%	CRT_G
16	PCH_CRT_B	PCH_CRT_B	R532	2	UMA ONLY@	0.0402_5%	CRT_B
16	PCH_CRT_HSYNC	PCH_CRT_HSYNC	R530	2	UMA ONLY@	0.0402_5%	CRT_HSYNC
16	PCH_CRT_VSYNC	PCH_CRT_VSYNC	R528	2	UMA ONLY@	0.0402_5%	CRT_VSYNC
16	PCH_CRT_CLK	PCH_CRT_CLK	R544	2	UMA ONLY@	0.0402_5%	CRT_DDC_CLK
16	PCH_CRT_DATA	PCH_CRT_DATA	R543	2	UMA ONLY@	0.0402_5%	CRT_DDC_DATA

PCH DDC PU 2.2K on Page 17

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Size B	Document Number	NEW71/91 M/B LA-5893P Schematic <sup>0.1</sup>		Date	Rev
		Tuesday, December 22, 2009		Sheet 29	of 56



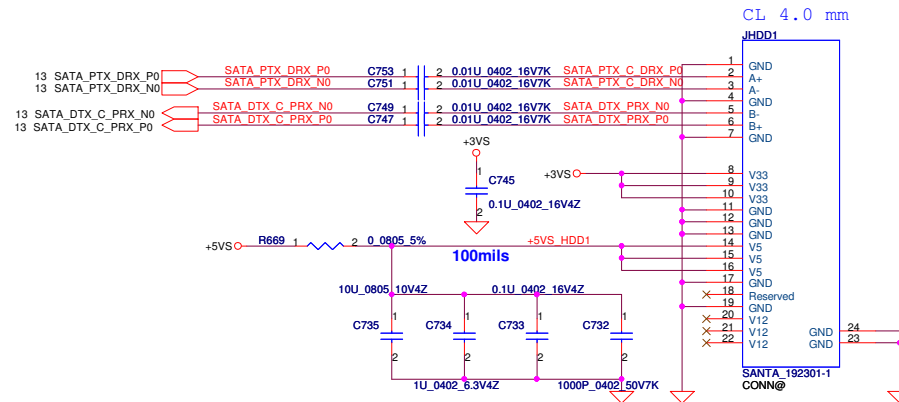
EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

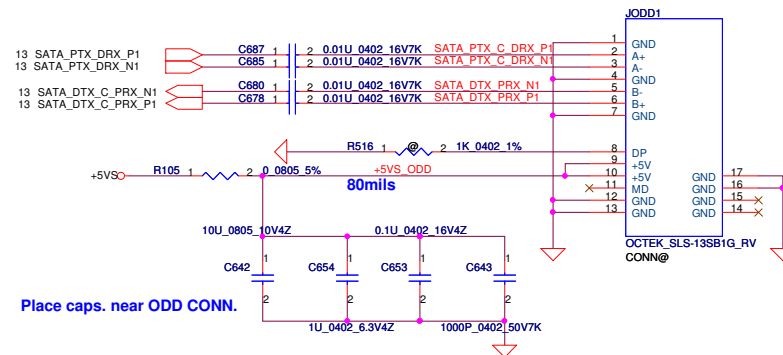
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	
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Size	Document Number	Rev		NEW71/91 M/B LA-5893P Schematic	
Custom	NEW71/91 M/B LA-5893P Schematic	Date		Tuesday, December 22, 2009	
Sheet		30		of 56	

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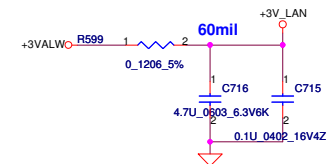
**SATA HDD1 Conn.**



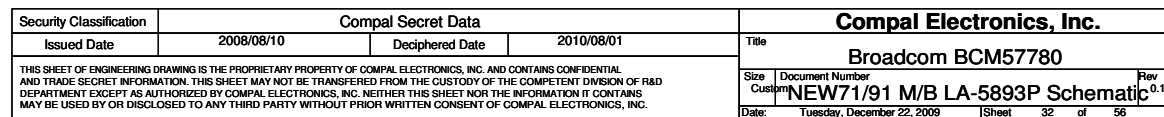
**SATA ODD Conn.**



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				Customer	NEW71/91 M/B LA-5893P Schematic
				Rev	0.1
Date:	Tuesday, December 22, 2009	Sheet	31	of	56

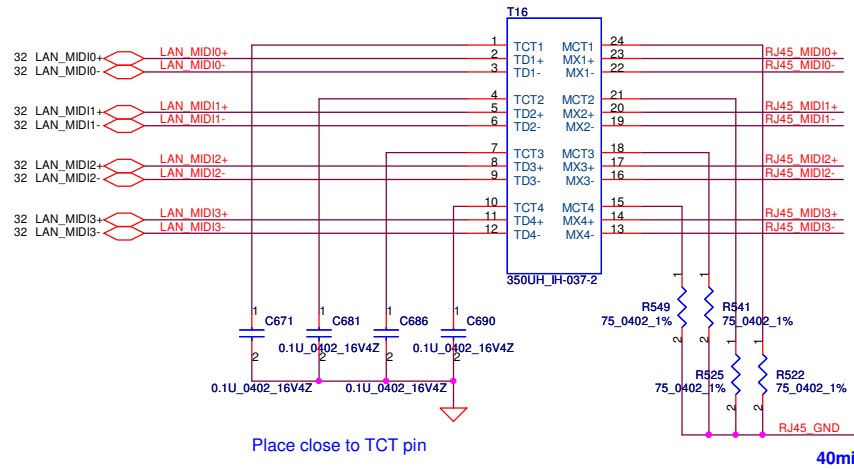


	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

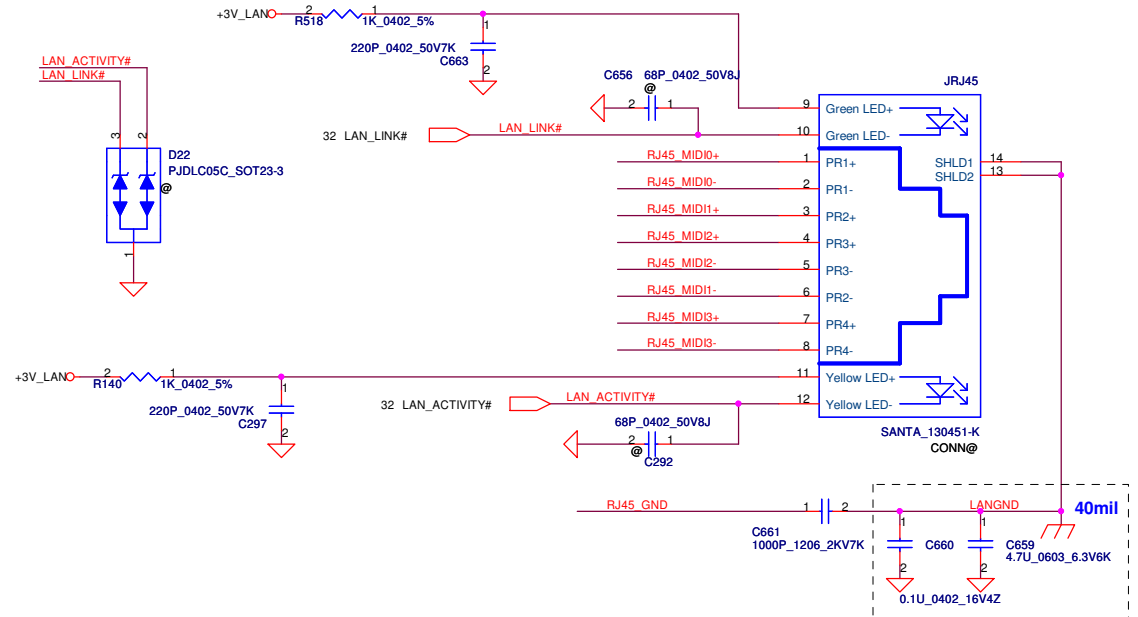




## LAN Connector

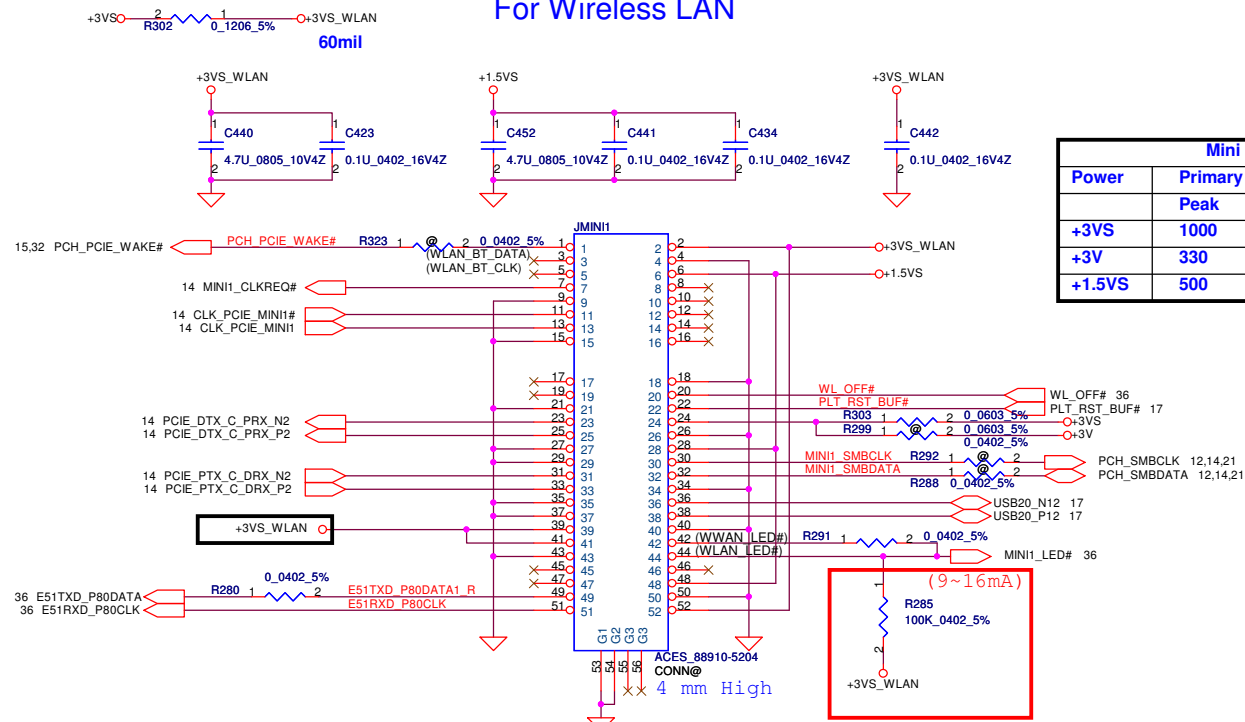


BOTHHAND: S X'FORM\_ GST5009-D LF LAN, SP050006B00  
TIMAG:S X'FORM\_ IH-160 LAN , SP050006F00



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				Custm	NEW71/91 M/B LA-5893P Schematic	0.1	
				Date:	Tuesday, December 22, 2009	Sheet 33 of 56	

## For Wireless LAN



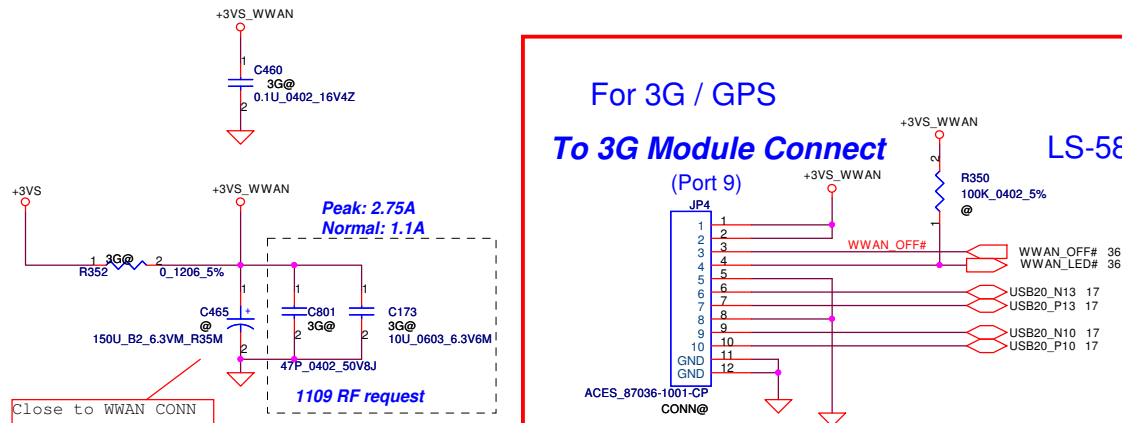
Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

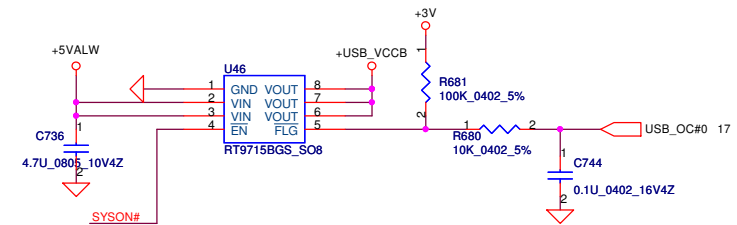
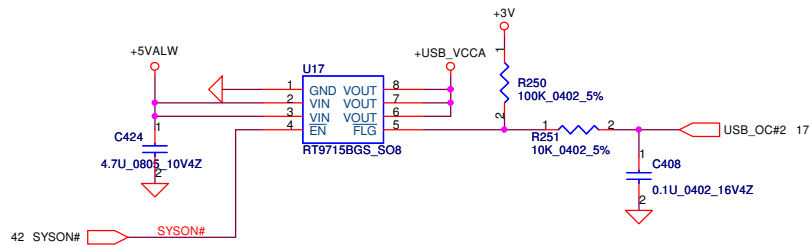
## For 3G / GPS

To 3G Module Connect

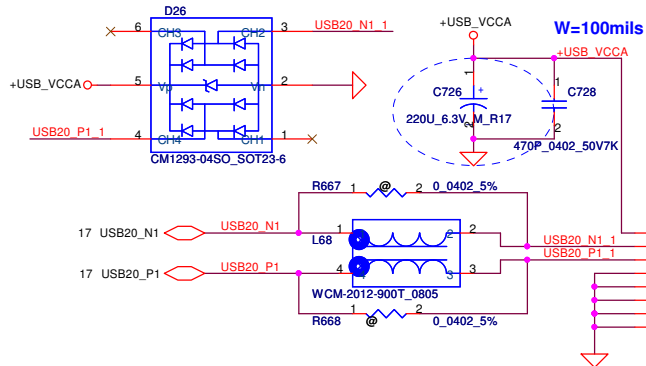
LS-5895



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Size	Document Number	Customer	NEW71/91 M/B LA-5893P Schematic	Rev	0.1
Date:	Tuesday, December 22, 2009	Sheet	34	of	56



2009/08/14 CHANGE cap

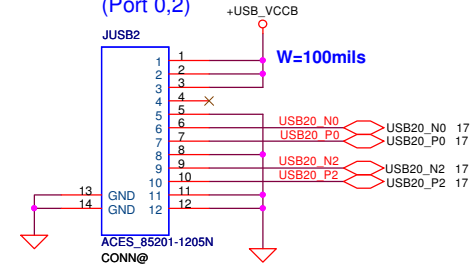


2009/08/25 Update Footprint(follow NAL00)

### USB Conn. (Port 1)

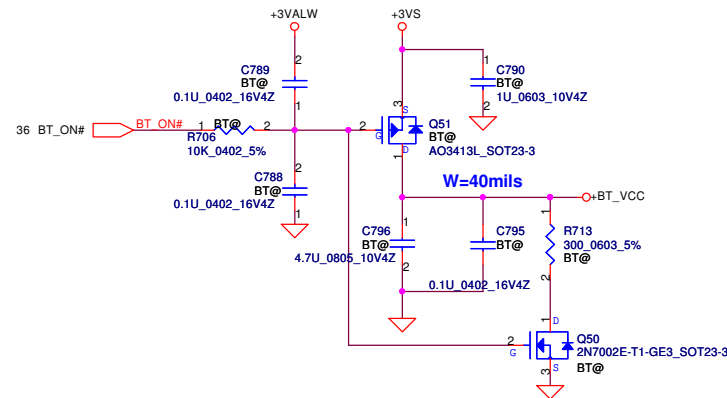
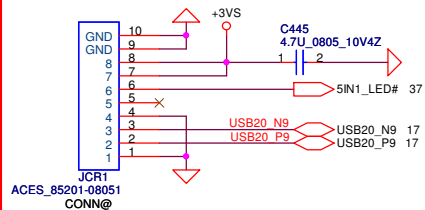
SUYIN\_020133GB004M51PZR  
CONN@

### USB/B Conn. LS-5891 (Port 0,2)

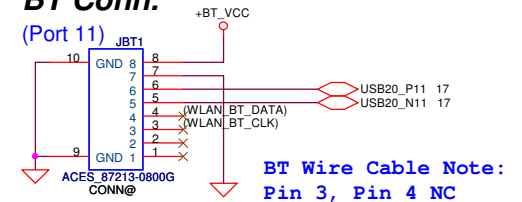


2009/08/24 CHANGE Conn to FFC Type

### Card Reader Conn. LS-5896



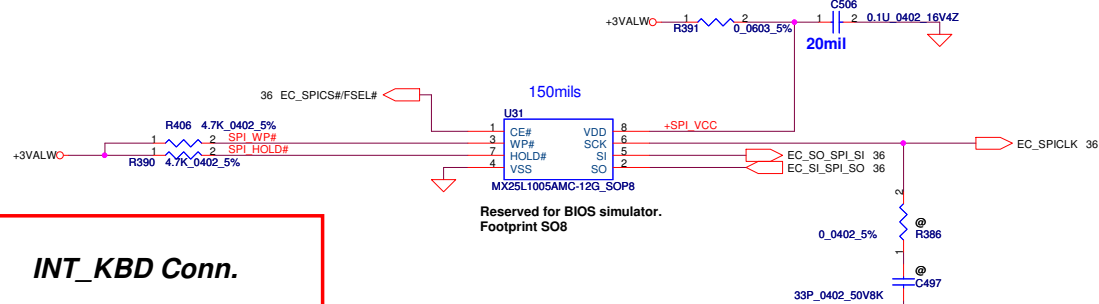
### BT Conn. (Port 11)



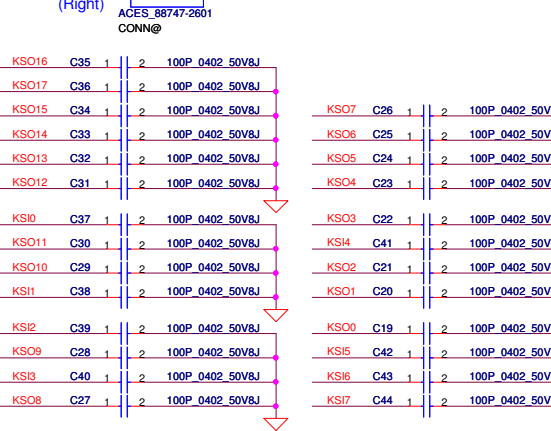
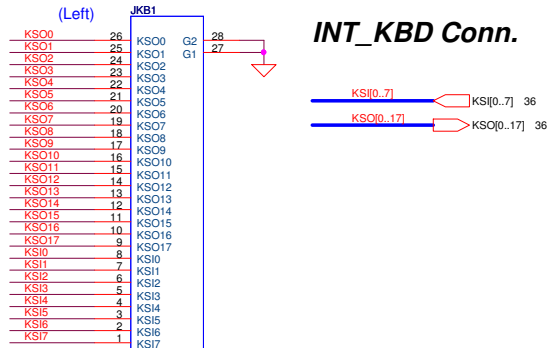
BT Wire Cable Note:  
Pin 3, Pin 4 NC

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2010/08/01				Title				USB / BT / USBB			
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				Customer				NEW71/91 M/B LA-5893P Schematic			
				Date				Thursday, December 24, 2009			
				Sheet				35 of 56			



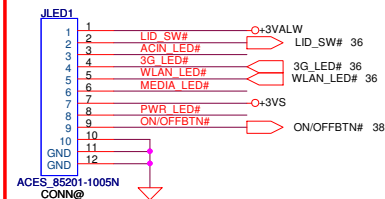


## INT\_KBD Conn.

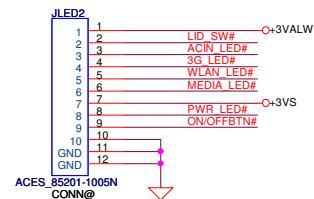


## LS-5893+LS-5894(Lid Board)

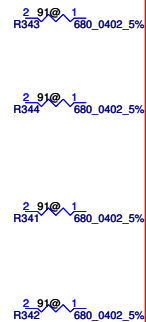
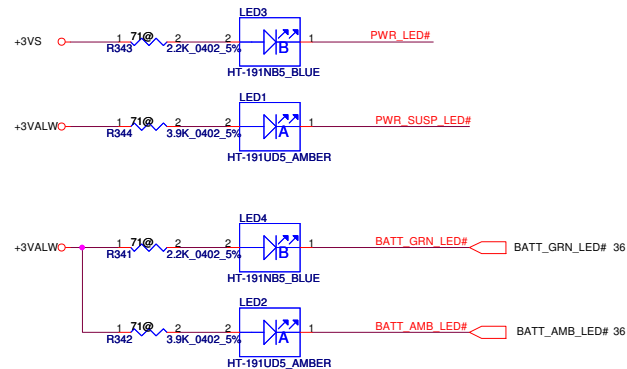
### LED/B RIGHT (90)



### LED/B LEFT (70)

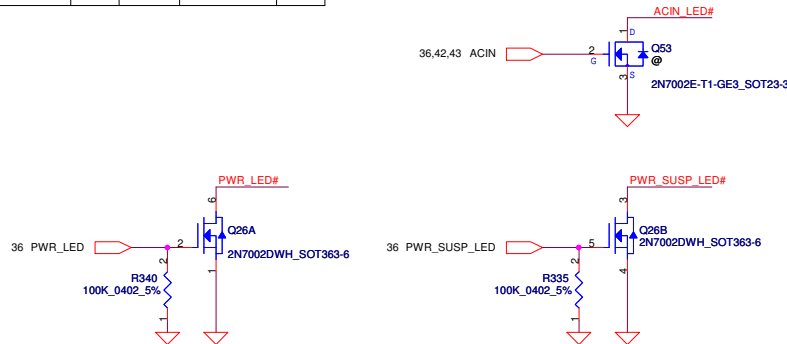
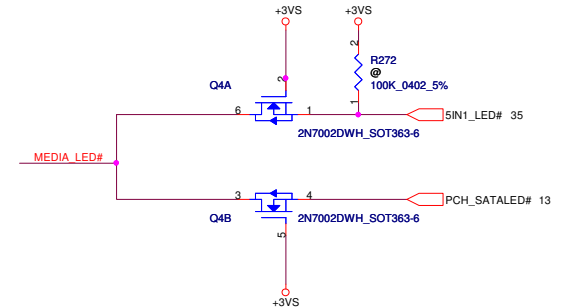
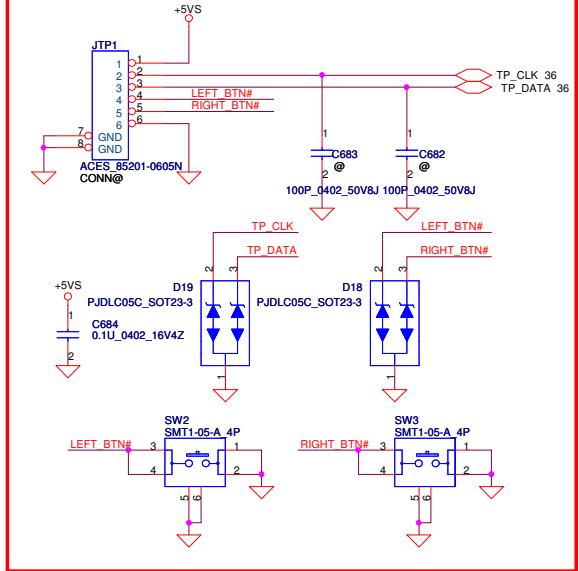


LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		



Bom option  
For 71 and 91

## To TP/B Conn.

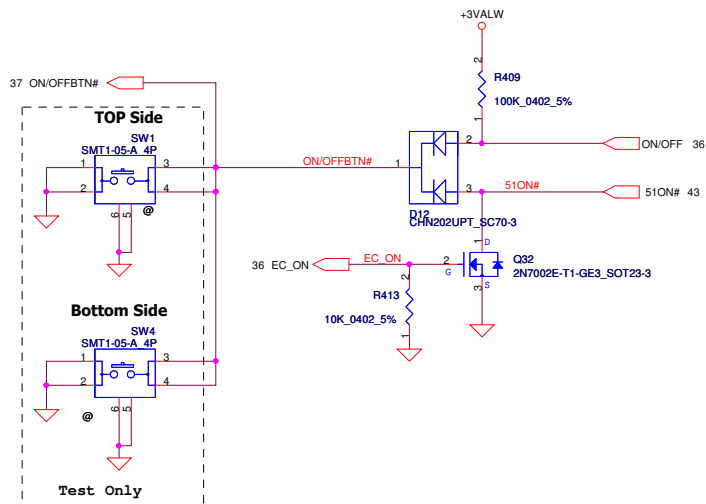


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Size	B	Document Number	NEW71/91 M/B LA-5893P Schematic	Rev	0.1
Date:	Tuesday, December 22, 2009	Sheet	37	of	56

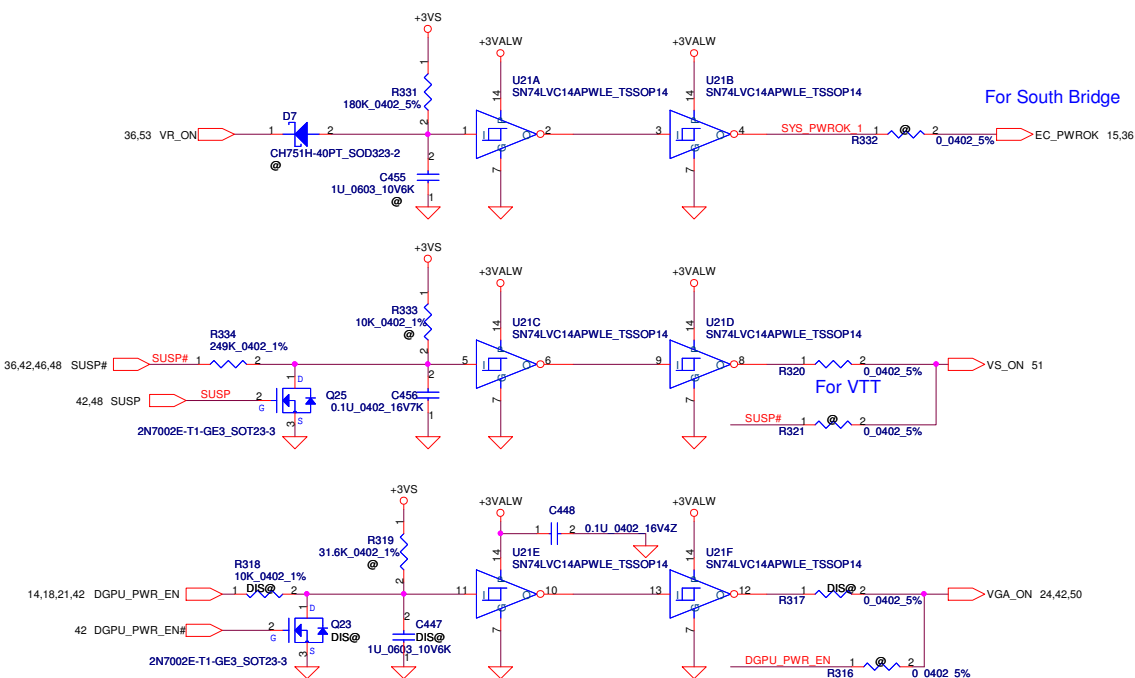


## Power Button

ON/OFF switch

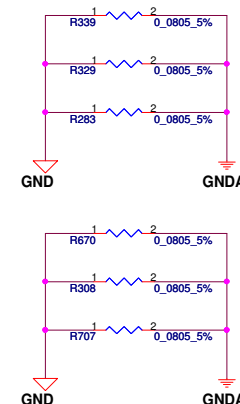
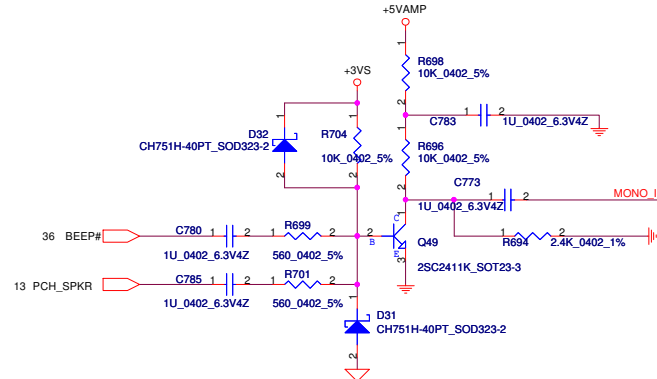
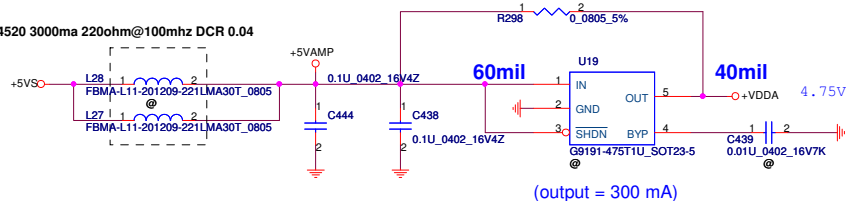


## Power ON Circuit



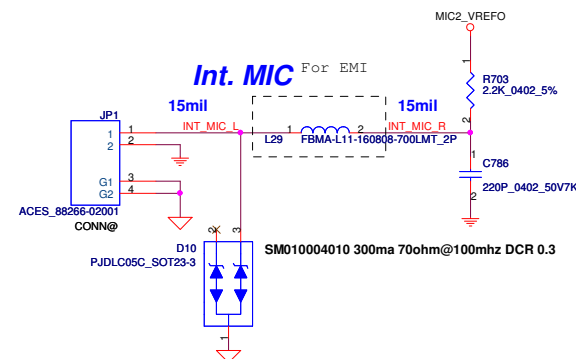
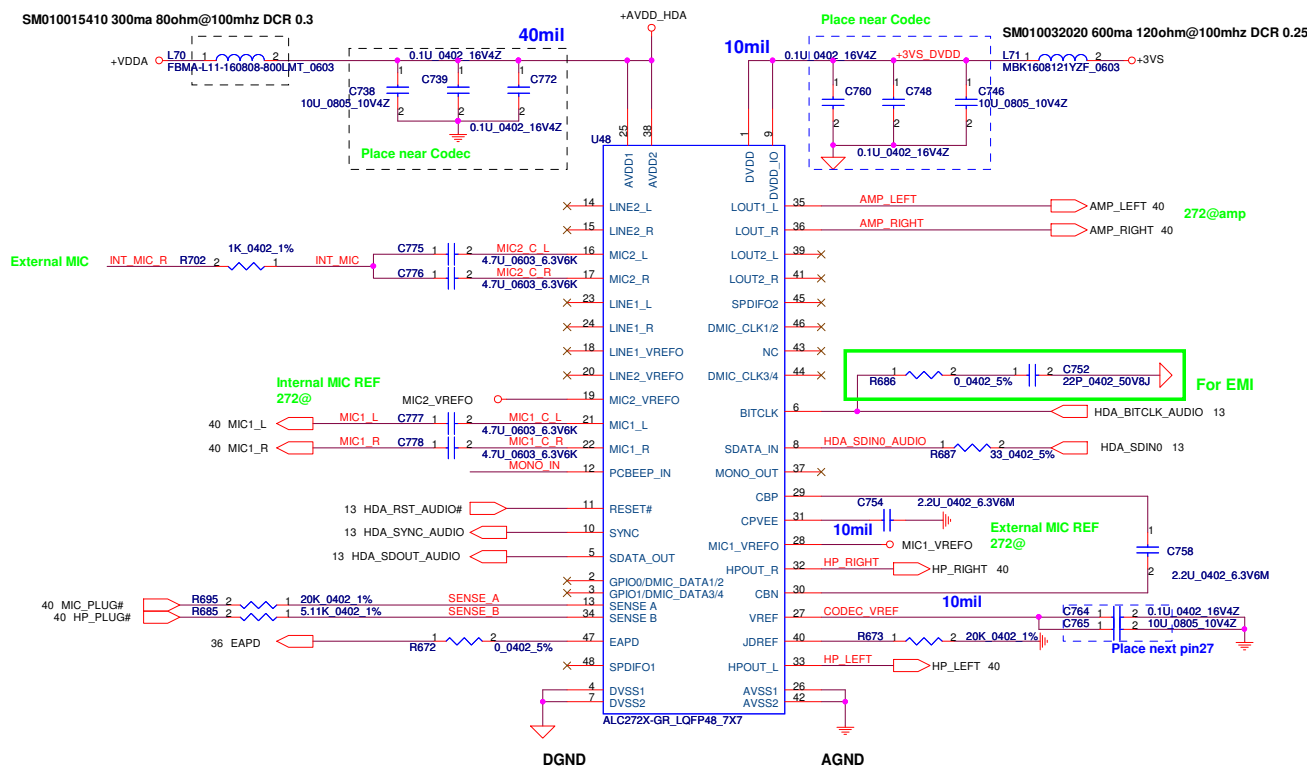
Security Classification		Compal Secret Data				Compal Electronics, Inc.										
Issued Date		2008/08/10		Deciphered Date		2010/08/01		Title								
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								Size B	Document Number			NEW71/91 M/B LA-5893P Schematic			Rev	
																0.1
								Date: Tuesday, December 22, 2009								Sheet 38 of 56

SM010014520 3000ma 220ohm@100mhz DCR 0.04



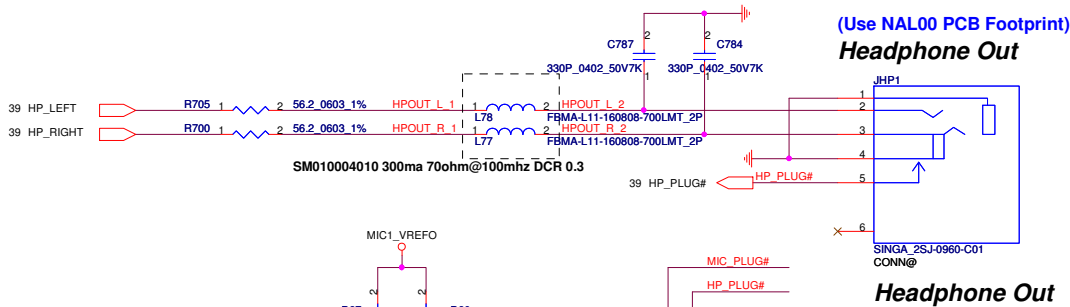
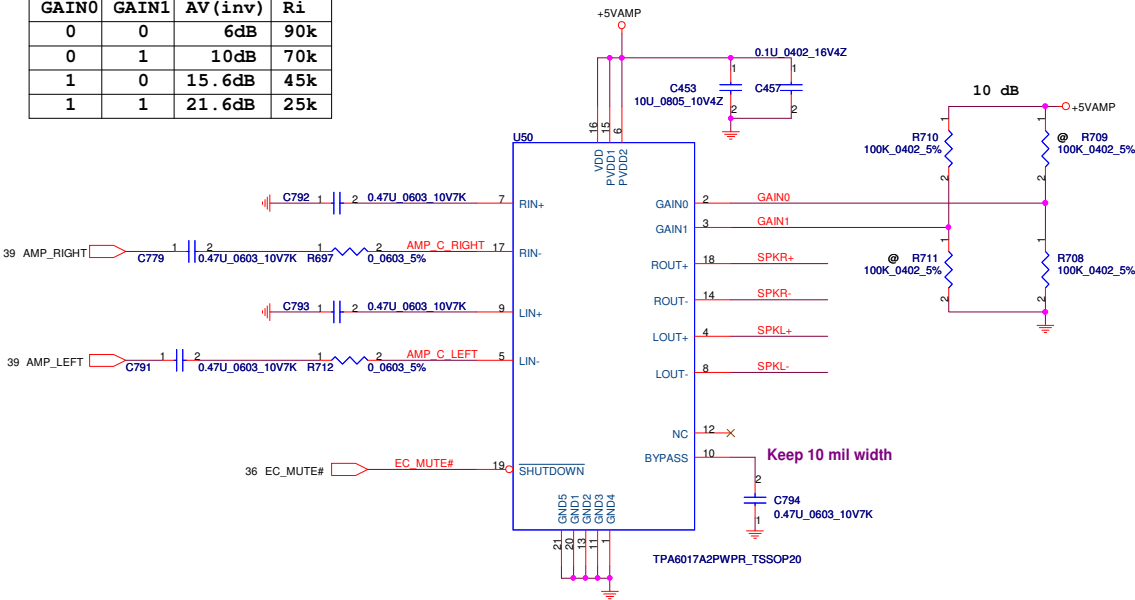
## HD Audio Codec

SM010015410 300ma 80ohm@100mhz DCR 0.3

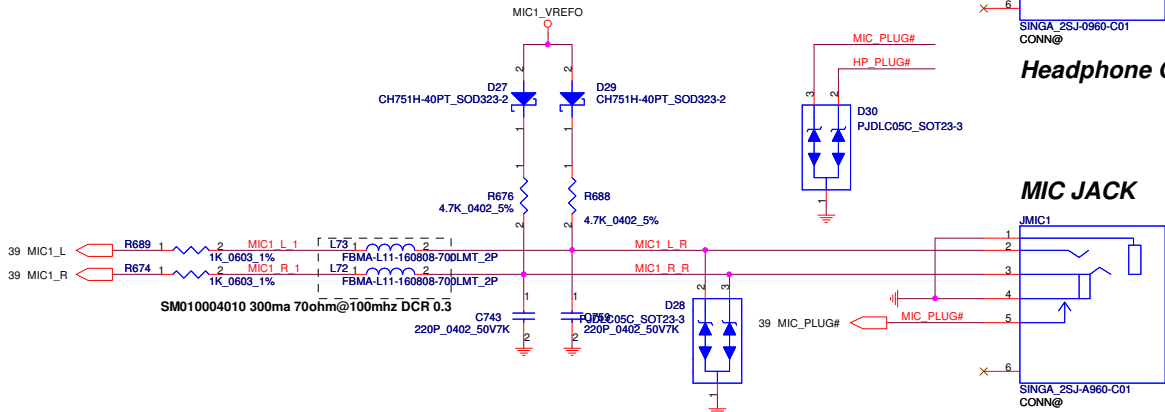
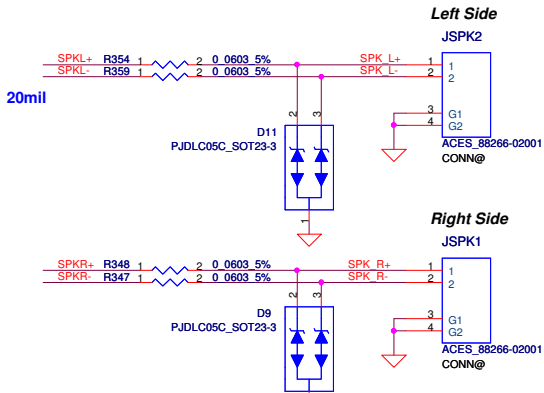


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Deciphered Date				2010/08/01				HD Audio Codec ALC272X			
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				Custom: NEW71/91 M/B LA-5893P Schematic				Rev 0.1			
				Date: Tuesday, December 22, 2009				Sheet 39 of 56			

GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

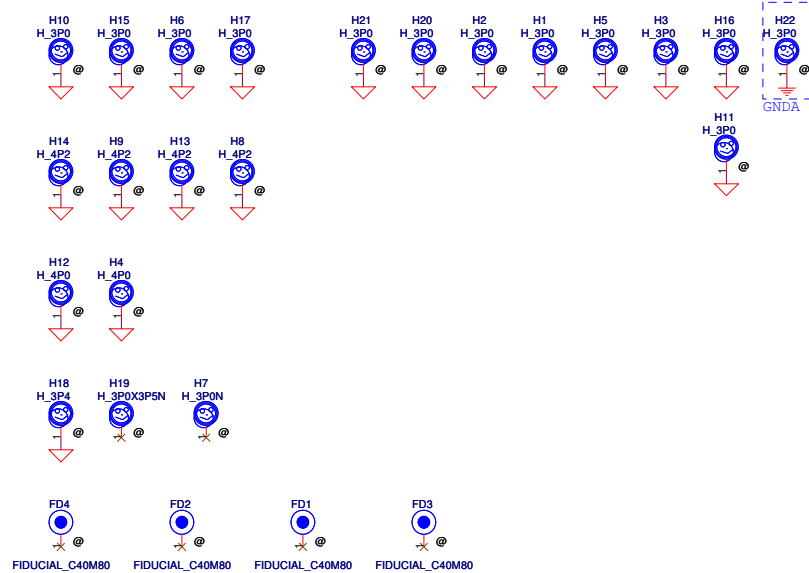
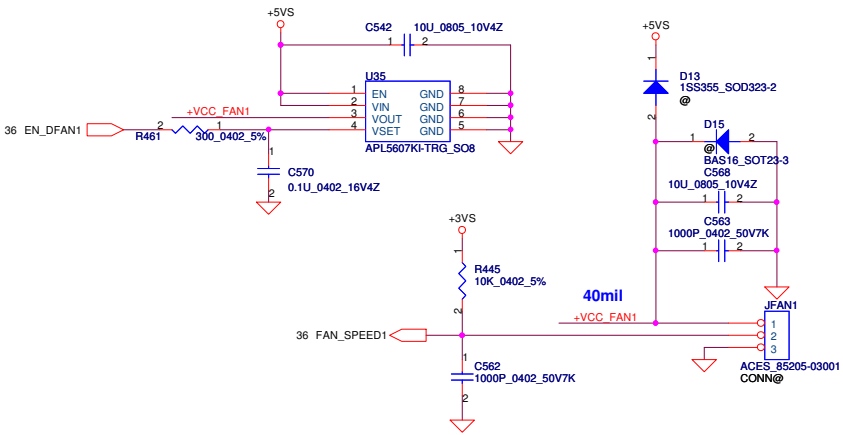


Int. Speaker Conn.

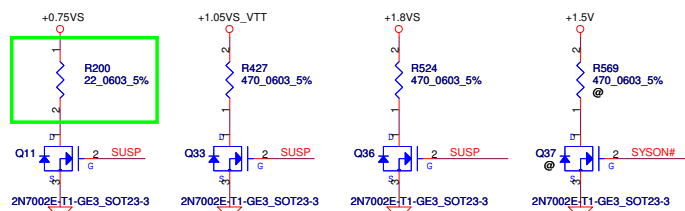
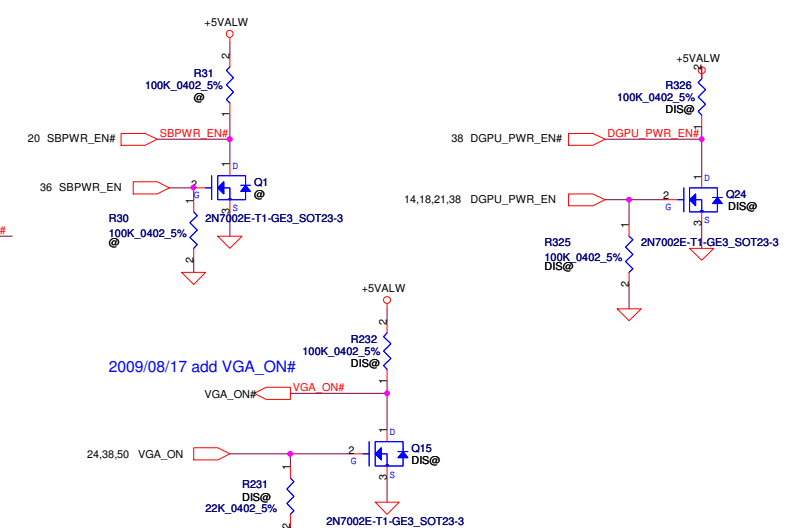
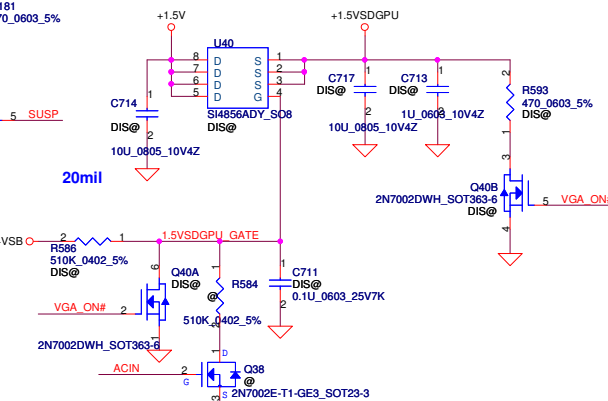
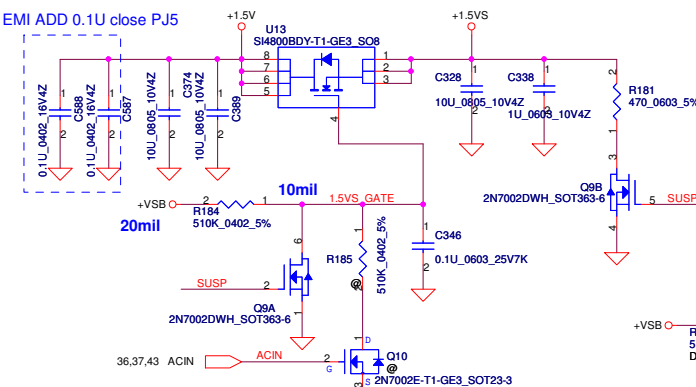
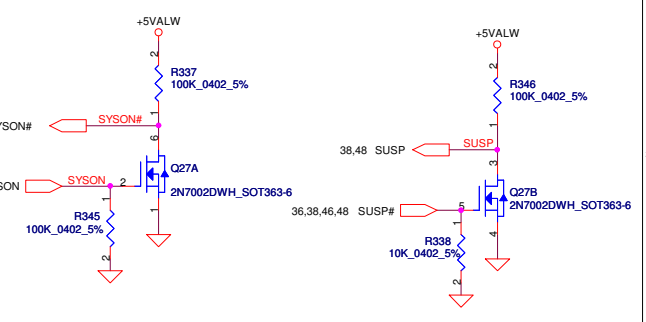
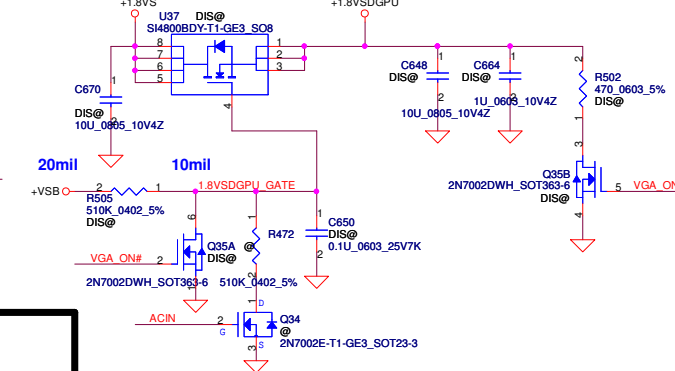
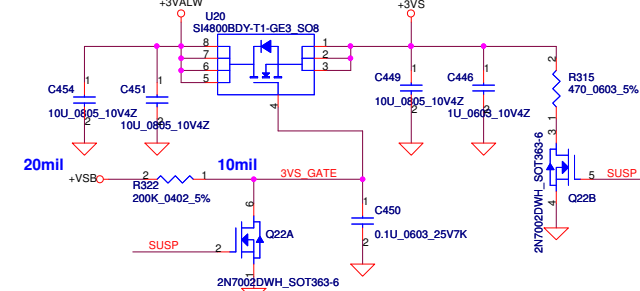
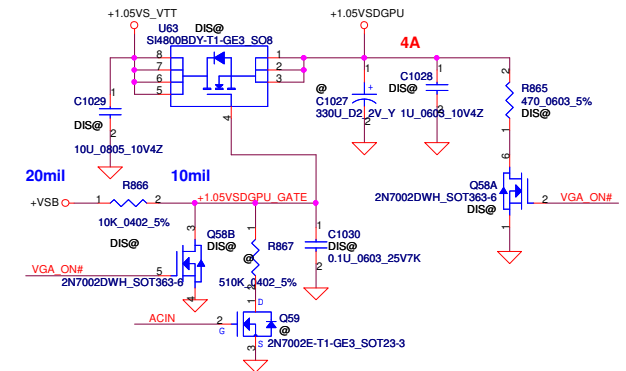
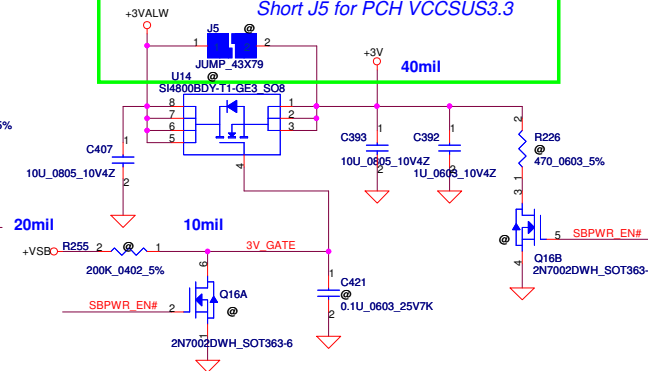
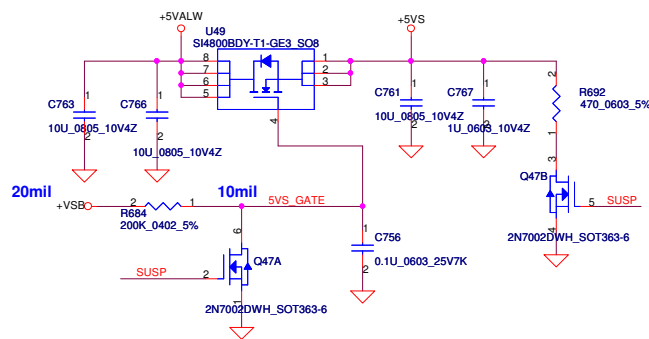


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				Date				Tuesday, December 22, 2009			
								Sheet 40 of 56			

FAN1 Conn



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								FAN & Screw Hole				
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						B	NEW71/91 M/B LA-5893P Schematic		0.1			
						Date:	Tuesdav. December 22, 2009		Sheet	41	of	56

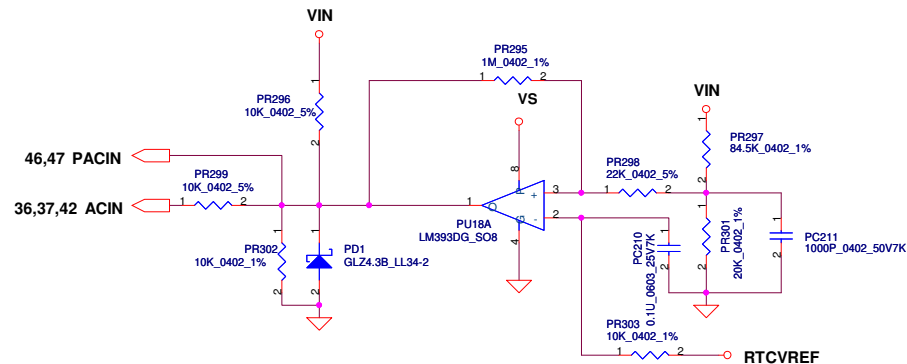
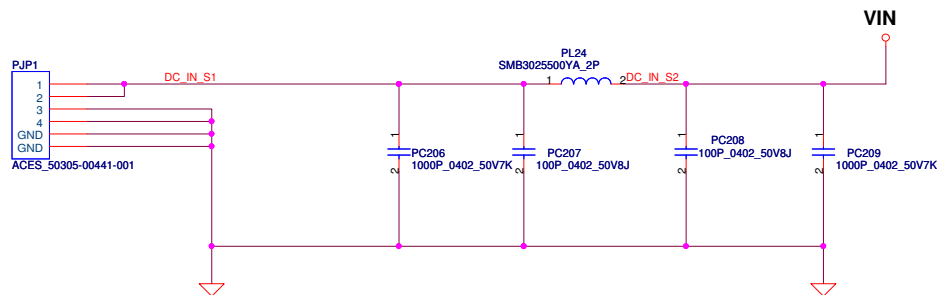


White Paper Rev.0.9  
0.75% Speed up discharg

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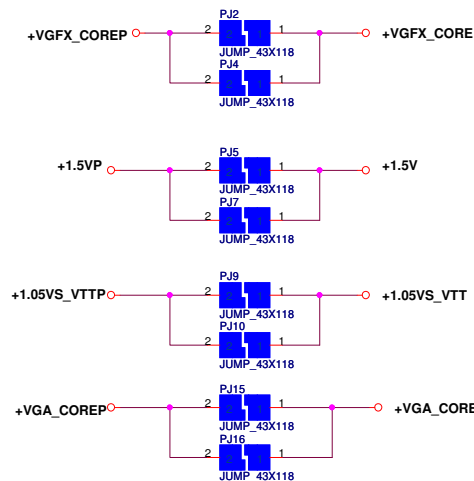
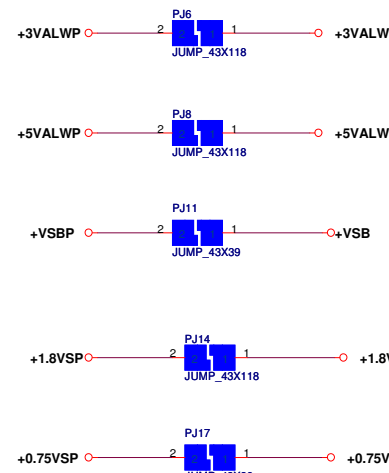
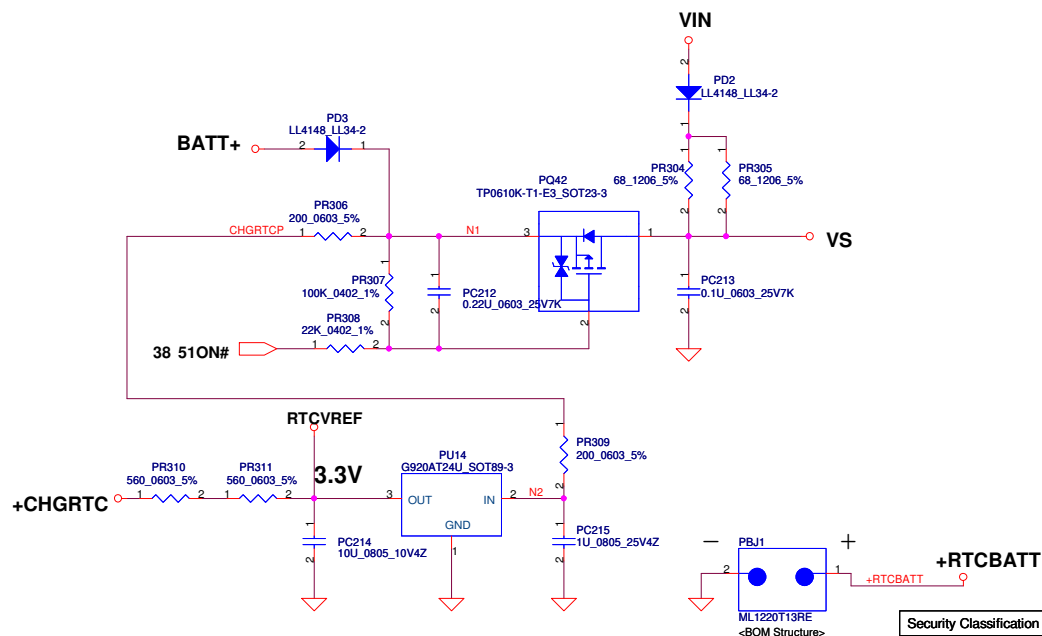
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				NEW71/91 M/B LA-5893P Schematic		0.1	
				Date	Tuesday, December 22, 2009	Sheet	42 of 56



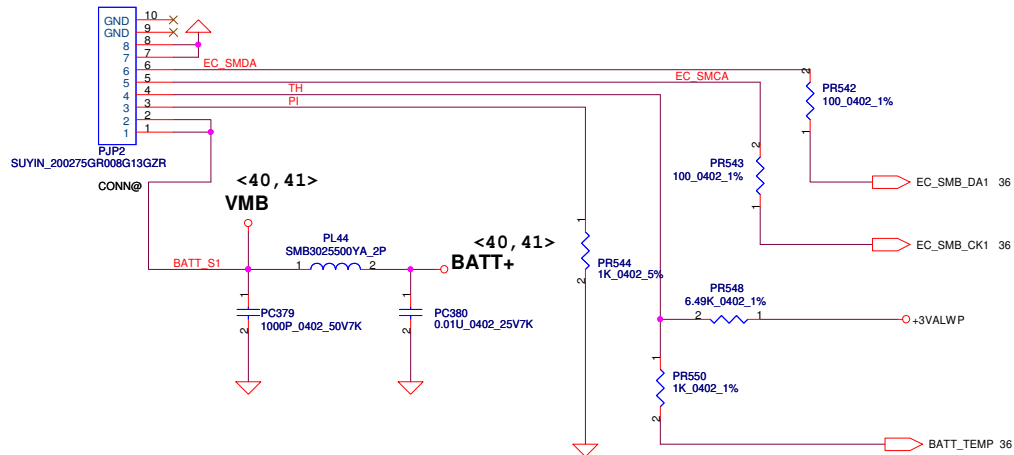


### Vin Dectector

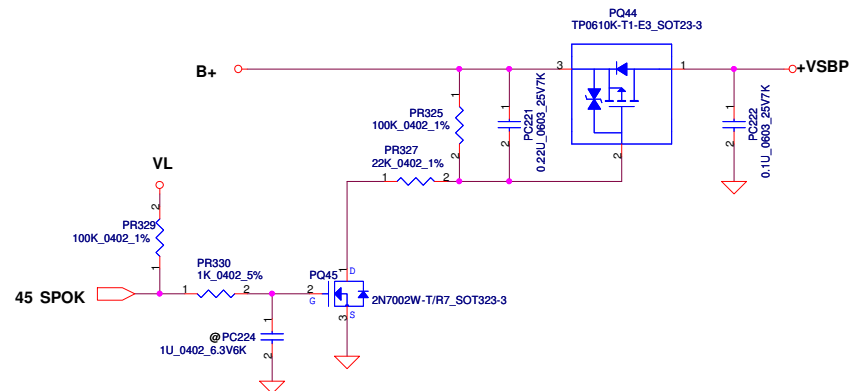
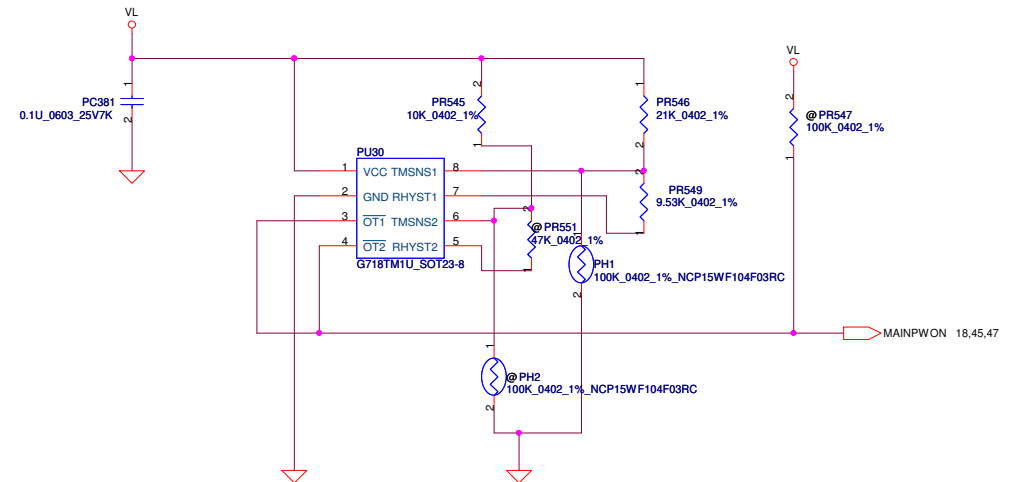
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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						Size	Document Number			NEW71		Rev
						Custom						0.1
						Date:	Tuesday, December 22, 2009		Sheet	43	of	56



PH1 under CPU botten side :  
CPU thermal protection at 92 degree C



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Issued Date		2007/09/20		Title	
		Deciphered Date		BATTERY CONN / OTP	
				Size	
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				Rev	
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				Date:	
				Tuesday, December 22, 2009	
				Sheet	
				44 of 56	

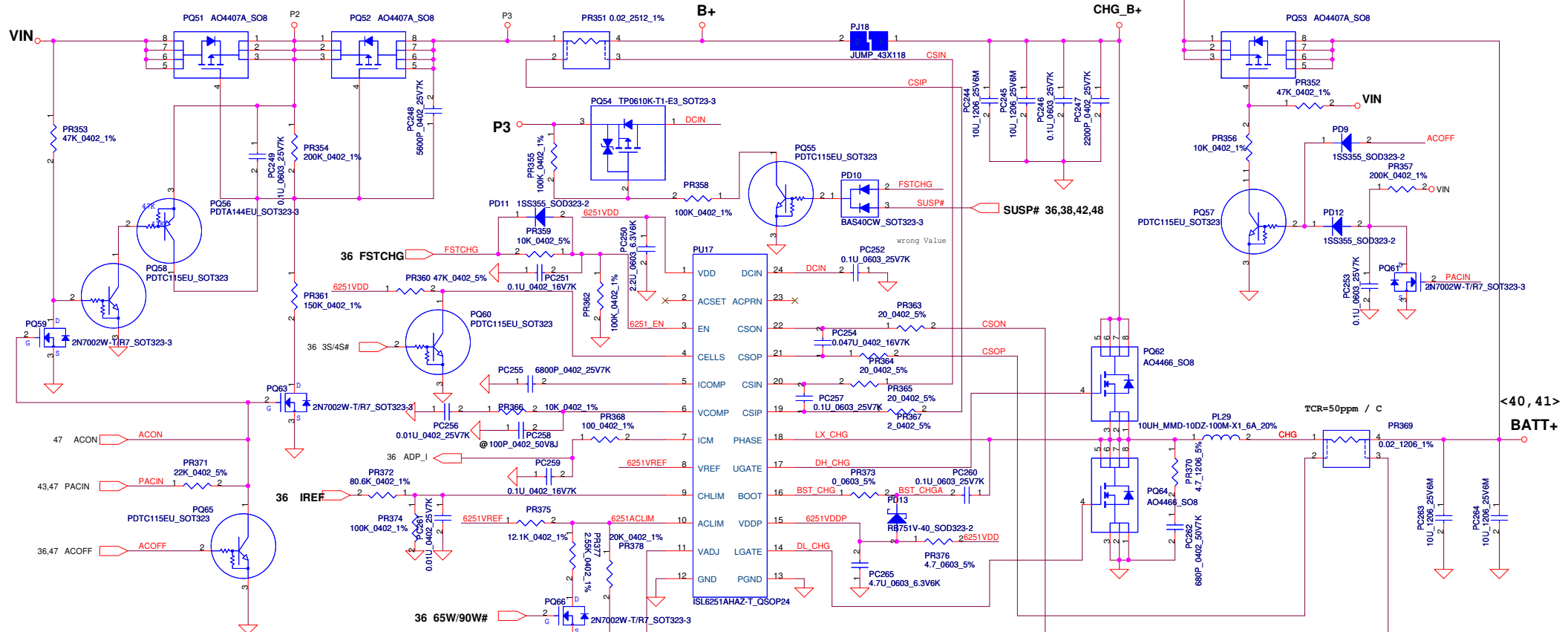
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Iada=0~4.74A (90W/19V=4.736A)  
Iada=0~3.42A (90W/19V=3.421A)

ADP\_I = 19.9\*Iadapter\*Rsense

CP = 85%\*Iada ; CP = 4.07A  
CP = 85%\*Iada ; CP = 2.91A



CP mode  
Iinput=(1/0.02) (0.05\*Vaclm/2.39+0.05)  
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A  
Iref=0.7224\*Icharge  
KI=0.7224  
IREF=0.43V~3.24V

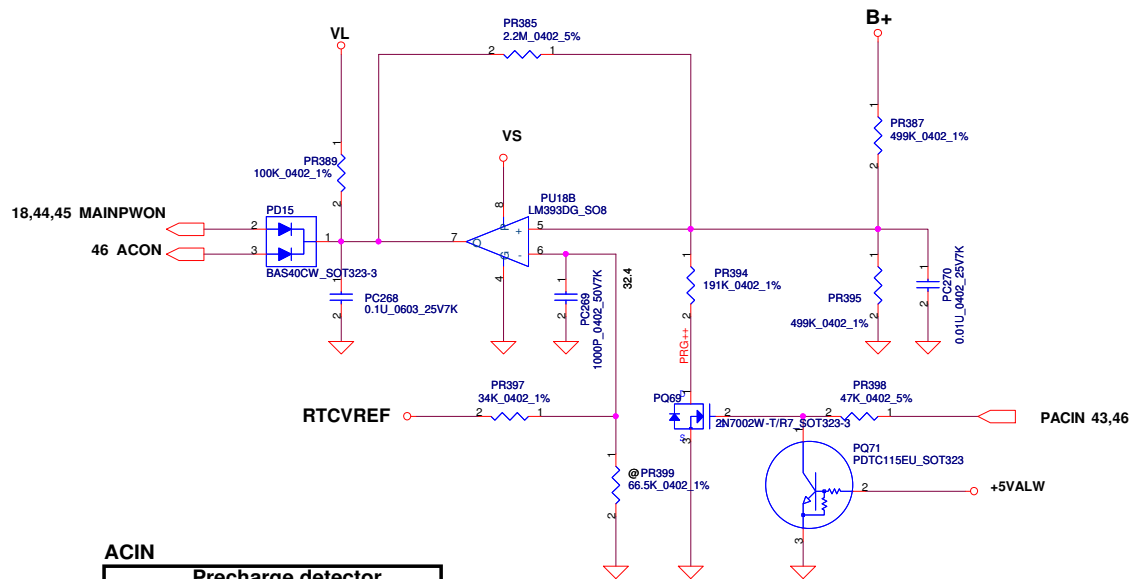
K1  
Vchlim=Iref\*(PR374/(PR372+PR374))  
=Iref\*(100K/(80.6K+100K))  
=Iref\*0.5537  
Icharge=(165mV/PR369)\*(Vchlim/3.3V)  
=(165mV/20m)\*(1/3.3V)\*Iref\*0.5537  
=1.3842\*Iref  
Iref=0.7224\*Icharge =>KI=0.7224

Kv  
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K  
R=514K//31.6K/(15.4K+31.6K)=1.372K  
r=514K/(514K//31.6K+28.14K)  
Vocell=0.175\*Vadj+3.99V  
4.2V=0.175\*Vadj+3.99V =>Vadj=1.2V  
Vadj=Vref\*(R/(R+514K))+CALIBRATE\*(r/(r+514K))  
1.1463=CALIBRATE\*0.6046 =>CALIBRATE=1.899  
1.899=(4.2-(Vocell+0.175))\*Kv=(4.2-(4.2+0.175))\*Kv  
A=Vref\*(R/(R+514K))=0.052  
Kv=9.451

LI-3S :13.5V---BATT-OVP=1.5012V  
BATT-OVP=0.1112\*VMB  
Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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Custom				0.1	
Date:	Tuesday, December 22, 2009	Sheet	46	of 56	



#### ACIN

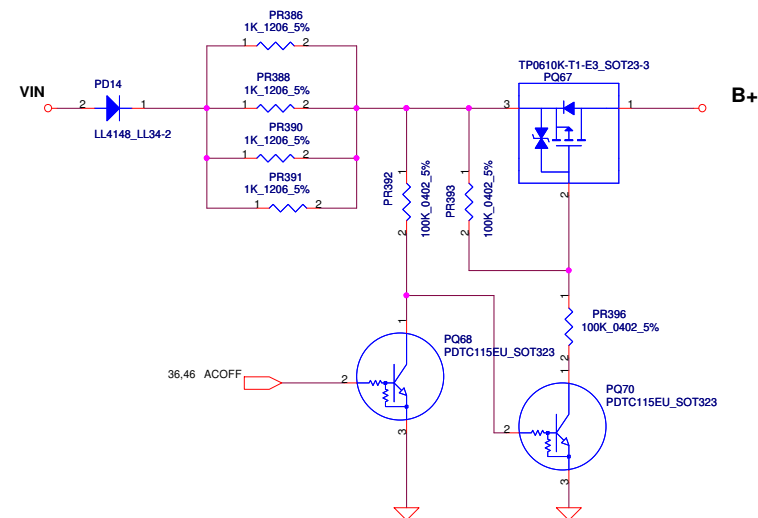
##### Precharge detector

	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

#### BATT ONLY

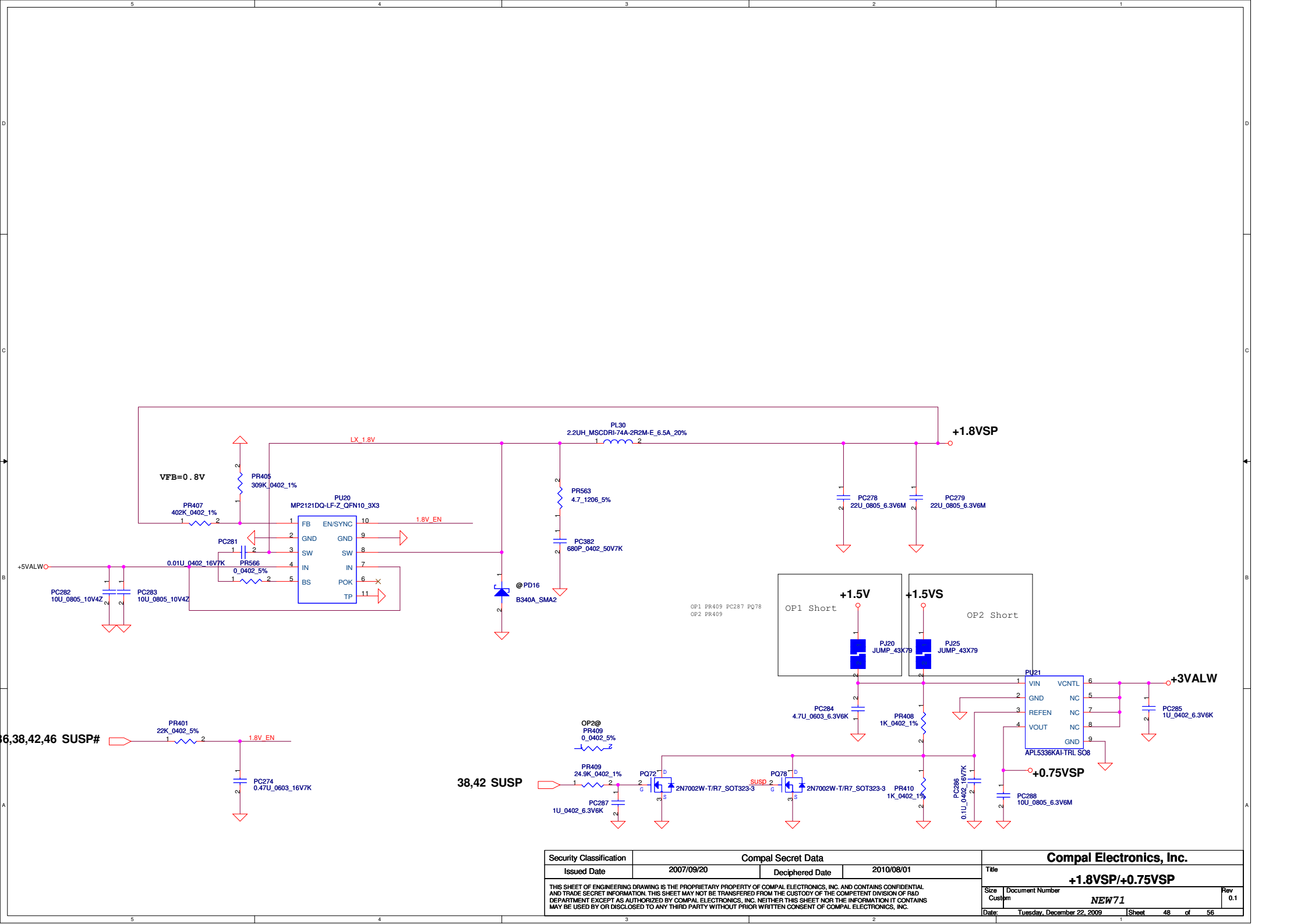
##### Precharge detector

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



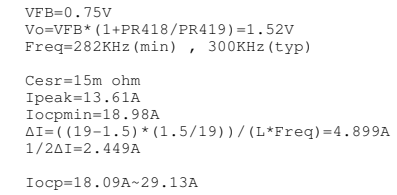
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				Date:	Tuesday, December 22, 2009	Sheet 47 of 56



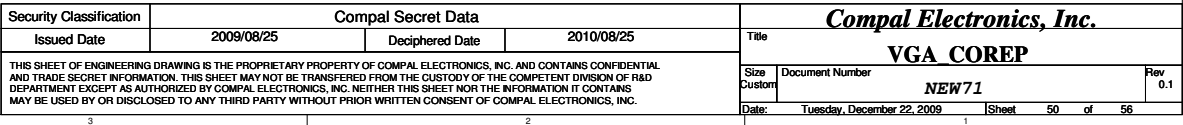


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Size	Custom	Document Number	NEW71		Rev
Date		Tuesday, December 22, 2009	Sheet	48	of 56

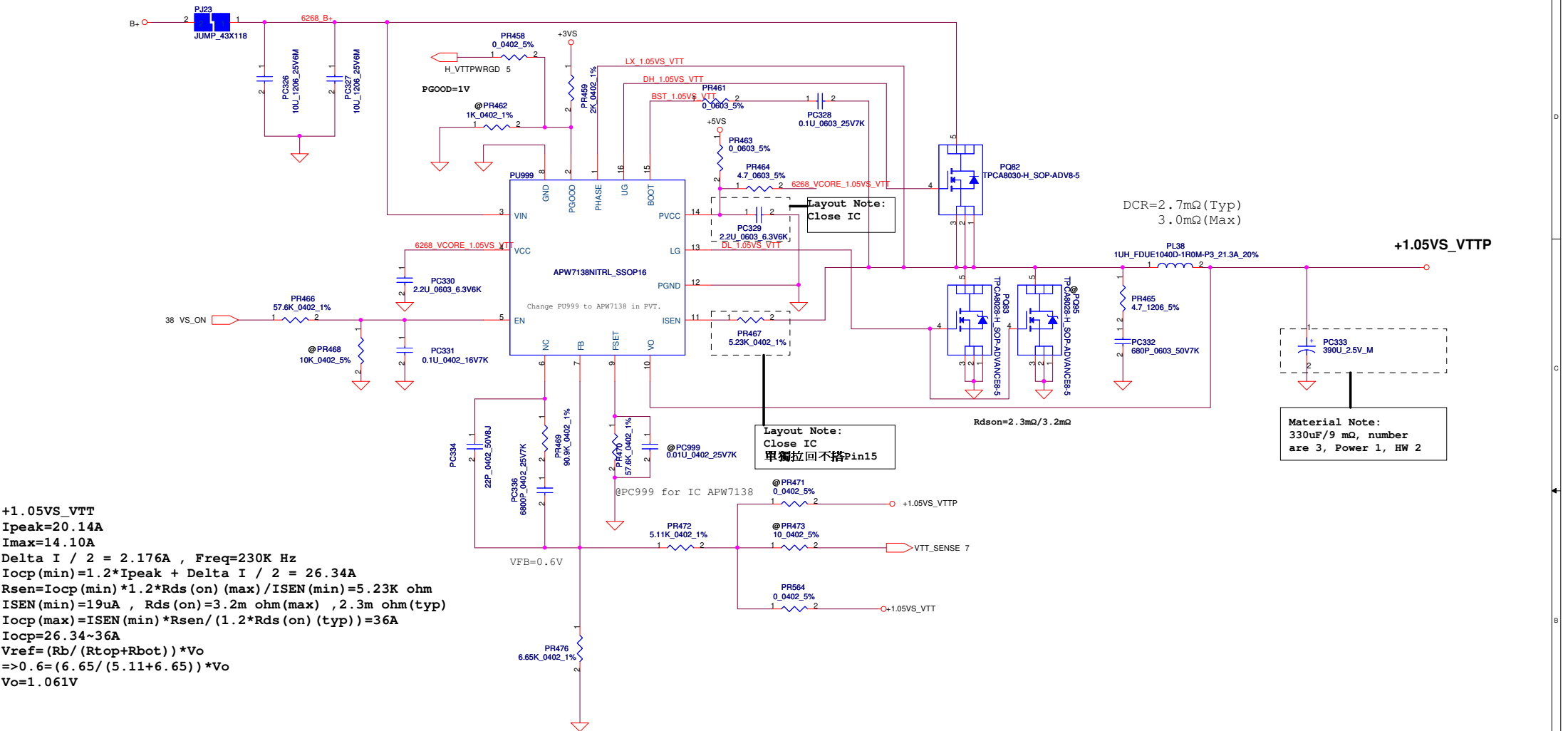
Because +1.5VSP has 17.74A power budget, it includes DDR3, VGA chip, VRAM, so must use molding choke.



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+1.05VS\_VTT  
Ipeak=20.14A  
Imax=14.10A  
Delta I / 2 = 2.176A , Freq=230K Hz  
Iocp(min)=1.2\*Ipeak + Delta I / 2 = 26.34A  
Rsen=Iocp(min)\*1.2\*Rds(on)(max)/ISEN(min)=5.23K ohm  
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) , 2.3m ohm(typ)  
Iocp(max)=ISEN(min)\*Rsen/(1.2\*Rds(on)(typ))=36A  
Iocp=26.34~36A  
Vref=(Rb/(Rtop+Rbot))\*Vo  
=>0.6=(6.65/(5.11+6.65))\*Vo  
Vo=1.061V



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					+1.05VS_VTTP
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				Document Number	0.1
				Customer	NEW71
				Date:	Tuesday, December 22, 2009
				Sheet	51 of 56

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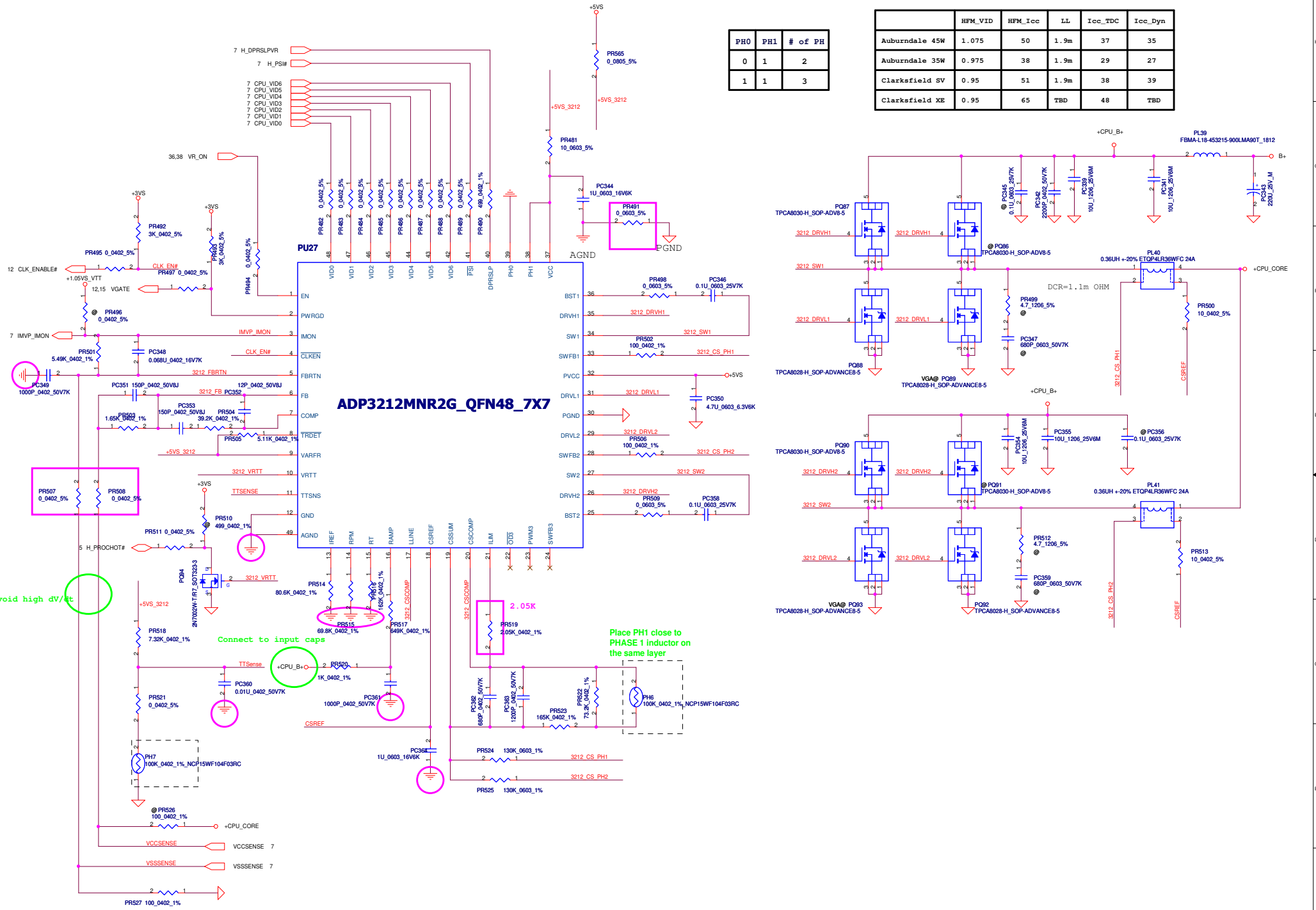
A

PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD

# ADP3212MNR2G\_QFN48\_7X17

Place PH1 close to PHASE 1 inductor on the same layer





## Version change list (P.I.R. List)

Page 1 of 3  
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	For BOM unique.	For BOM unique.	0.1	46	Change PD8 from SC1SS355003(S DIO 1SS355) to SC100001K00( DIO 1SS355 SOD323 T/R-5K)	2009-1021	to DVT
2	For BOM unique.	For BOM unique.	0.1	54	Delete PQ86/PQ91 SB00000HL00(S TR TPCA8030-H 1N SOP). Add PQ87/PQ90 SB00000HL00(S TR TPCA8030-H 1N SOP).	2009-1021	to DVT
3	For UMA Arrandale CPU commond design.	For UMA Arrandale CPU, we just only pop 1 HS MOS and 1 LS MOS.	0.1	54	Delete PQ89/PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
4	For VTT Power rail commond design.	For VTT Power rail commond design, we pop 1 HS MOS and 1LS MOS.	0.1	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
5	CIS link error.	CIS link error.	0.1	54	Change PR500 from SD028100A00(S RES 1/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1021	to DVT
6	BOM unique.	BOM unique.	0.1	47	Chnage PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
7	BOM unique.	BOM unique.	0.1	49	Chnage PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
8	BOM unique.	BOM unique.	0.1	54	Chnage PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
9	BOM unique.(For Madison/Park SKU)	BOM unique.(For Madison/Park SKU)	0.1	52	Chnage PC367 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
10	BOM unique.	BOM unique.	0.1	46	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
11	BOM unique.	BOM unique.	0.1	54	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206) Change PC354/PC355 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
12	+1.05VS_VTTP Cost down 1 LS MOS. HW request.	+1.05VS_VTTP Cost down 1 LS MOS. Because +1.05VS_VTT has voltage drop issue, HW request, remote sense to close to PCH.	0.2	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP ) Delete PR471 SD028000080(S RES 0 0402 5%) Delete PR473 from SD034100A80(S RES 10 0402 5%) Add PR564 SD028000080(S RES 1/16W 0 0402 5%)	2009-1029	to DVT
14	Adjust +1.05VS_VTTP OCP.	Because we remove a LS MOS, so OCP must adjust.	0.2	52	Change PR467 from SD000004080(S RES 1/16W 2.2K +-1% 0402) to SD034499180(S RES 1/16W 4.99K 0402 1%)	2009-1029	to DVT
15	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PU19 SA00001NC00 (S IC APL5913-KAC-TRL SO 8P)	2009-1029	to DVT
16	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PR402 SD034150280, PR404 SD034120280.	2009-1029	to DVT
17	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PC273 SE075103K80 PC275 SE000000I10 Delete PC272 SE107475K80, PC271 SE107105M80 Delete PR401 and PR403 SD028220280, PC274 SE026474K80	2009-1029	to DVT
18	+VGA_COREP, efficiency issue.	Increase Freq, decrease choke, to improve efficiency.	0.2	51	Change PR196 from SD034442280 to SD034365280. Change PL14 from SL200000V00 to SH000005680	2009-1029	to DVT
19	+VGA_COREP, OVP issue.	Becasue if PR199/PR202 pop 0ohm, it will cause OVP when VID change from 00 to 11)	0.2	51	Change PR199/PR202 from SD028000080 to SD028100280 (S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
20	+VGA_COREP, cost issue.	Cost down.	0.2	51	Change PQ75/PQ78 from SB00000GL00(S TR TPCA8028-H 1N SOP) to SB000009F80(S TR AO4456 1N SO8)	2009-1029	to DVT
21	+VGA_COREP, satndard design.	+VGA_COREP, satndard design, pop 1HS MOS and 2LS MOS, so remove one HS MOS PQ79.	0.2	51	Delete PQ79 SB000008L80 (S TR SI7686DP-T1-E3 1N POWERPAK SO8 )	2009-1029	to DVT
22	+GFX_COREP, spike issue.	Because +GFX_COREP has spike voltage issue, add schottky diode across GFXVR_EN and VS_ON to solve it.	0.2	51	Add PD17 SCS00000Z00 (S SCH DIO RB751V-40 SOD-323 )	2009-1029	to DVT
23	+VGA_COREP, OCP caaculation erroe issue.	Because VGA_CORE has 2 LS MOS, APW7138 detect LS Rdson, so when caculate OCP, Rdson must reduce 1/2.	0.2	51	Change PR190 from SD034649180 to SD034511180 (S RES 1/16W 5.11K 0402 1%)	2009-1029	to DVT

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				Date:	Tuesday, December 22, 2009
				Sheet	54 of 56
				Rev	0.1

A -->Modify item

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				Size Custom	Document Number NEW71/91 M/B LA-5891P Schematic
Date:		Friday, December 18, 2009		Sheet	55 of 56
				Rev	0.1

PCB  
ZZZ  
LA-5893P REV0 M/B

ZZZ1  
X7621@  
X76198BOL21  
ALT. GROUP PARTS 1G SAM

ZZZ2  
X7622@  
X76198BOL22  
ALT. GROUP PARTS 1G HYN

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		Size Custom	Document Number NEW70 M/B LA-5891P Schematic	Rev 0.1	
Date:		Monday, December 21, 2009		Sheet	56 of 56